Embedded Linux on FPGAs for fun and profit

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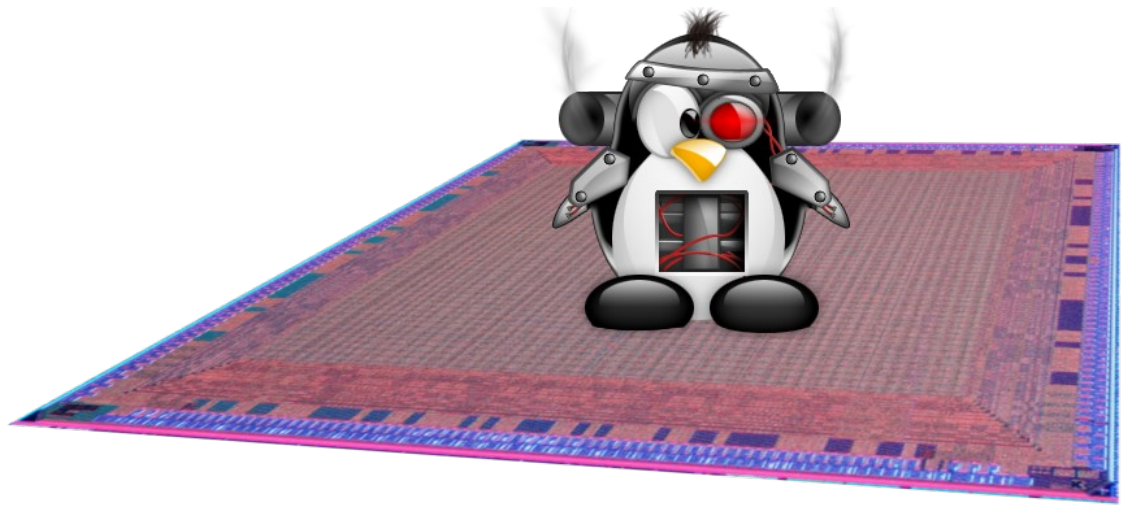

John Williams

CEO/CTO PetaLogix

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Thanks

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- EboxCreate for a great project and permission to talk about it
- The University of Queensland, Australia
- MicroBlaze/Linux community

Why this is so cool

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- Kernel hackers must ***respect*** computer architecture
- Embedded Linux hackers must ***understand*** computer architecture
- FPGA Linux hackers ***play God*** with computer architecture!

Agenda

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- FPGAs and Programmable SoC 101
- Linux on FPGAs - overview
- Case study - EBoxCreate EBC701
- MicroBlaze Linux status and roadmap
- Getting involved
- Q & A

FPGAs and System-on-Chip

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- What's an FPGA?
- Why are they so useful?
- How do we develop programmable SoC?
- FPGAs for the win
  - DSP / media processing
  - custom interfaces
  - rapid system prototyping / evolving requirements
  - defraying silicon costs over product lifetime

FPGAs 101 – the basics

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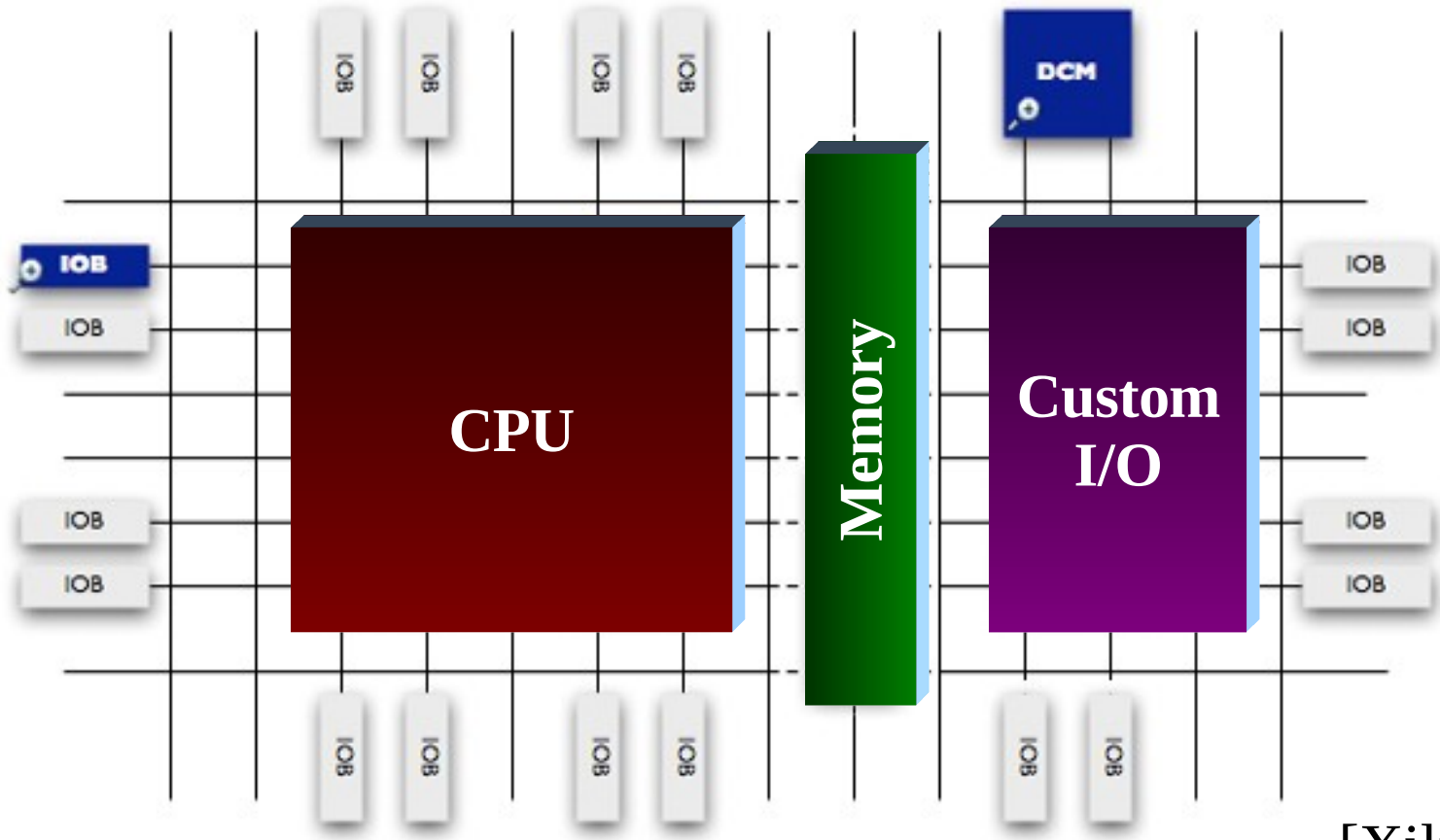

[Xilinx]

FPGAs 101 – IP Cores

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- IP Core
  - IP = Intellectual Property
  - Think of it as a hardware module or component
    - CPU, Ethernet MAC, memory controller, DSP, ...
    - but it lives inside the FPGA
- “Soft”
  - IP core implemented with FPGA logic resources
  - Any number of instantiations (to device capacity)
  - Parameterisable at FPGA synthesis-time
    - e.g. number of memory ports, HW checksum offload, ...

FPGAs 101 – IP Cores

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- Example of MicroBlaze CPU instantiation

```
BEGIN microblaze
 PARAMETER INSTANCE = microblaze_0
 PARAMETER HW_VER = 7.10.d
 PARAMETER C_USE_FPU = 0
 PARAMETER C_CACHE_BYTE_SIZE = 8192
 PARAMETER C_DCACHE_BYTE_SIZE = 8192
 PARAMETER C_ICACHE_BASEADDR = 0x24000000
 PARAMETER C_ICACHE_HIGHADDR = 0x27ffffff
 PARAMETER C_DCACHE_BASEADDR = 0x24000000
 PARAMETER C_DCACHE_HIGHADDR = 0x27ffffff
 PARAMETER C_USE_BARREL = 1
 PARAMETER C_USE_DIV = 1
...
```

FPGAs 101 – IP Cores

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- "Hard"
  - IP core implemented in die mask of the chip
    - Connects into FPGA fabric with standard routing resources
  - Configuration predetermined by FPGA vendor
    - "cheaper" and more efficient but less flexible
- Some examples
  - PowerPC 405/440 CPU in Xilinx FX series
  - Multichannel SDRAM / DDR controllers in new Spartan6
  - DSP blocks in all modern Xilinx FPGAs

Embedded Systems on FPGAs

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- Soft CPUs tend to look a bit the same
  - 32 bit RISC, small configurable caches
  - configurable ALUs
  - configurable system architecture
  - custom instruction/coprocessor interconnect
- Performance
  - depends on system complexity and FPGA family/speed grade
    - typically Fmax 80-150MHz

Embedded Systems on FPGAs

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- Open source options
  - OpenRISC
  - LEON and Rachael (Sparc clones)
- Generic CPUs tend to be bigger and slower than their commercial, vendor-tuned cousins
- Most commercial soft-CPUs tend to be black-boxes
  - licensed to target only that vendor's FPGAs
  - Lattice Mico32 is an exception

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Linux on FPGAs

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- Xilinx MicroBlaze + uClinux 2.4.x (2002), linux-2.6.x (2006)
  - MMU added 2008, Linux support in current distro
  - List and commercial support from **PetaLogix**
- Altera NIOS / NIOS2
  - MMU added 2008, no Linux support yet?
  - Commercial support from Microtronix
- Lattice Mico32
  - commercial support from Theobroma

Linux on FPGAs - scenarios

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- Interesting but not necessarily useful
  - FPGA + Linux just because you can
  - Standard CPU + ethernet + memory
    - off-the-shelf SoC chipset will always be faster, cheaper, lower power
- Interesting ***and*** useful
  - use the FPGA programmability
    - high performance processing in custom hardware
    - non-standard IO protocols and combinations
    - rapid system and architecture prototyping
  - our case study touches all three

Linux on FPGAs – scenarios

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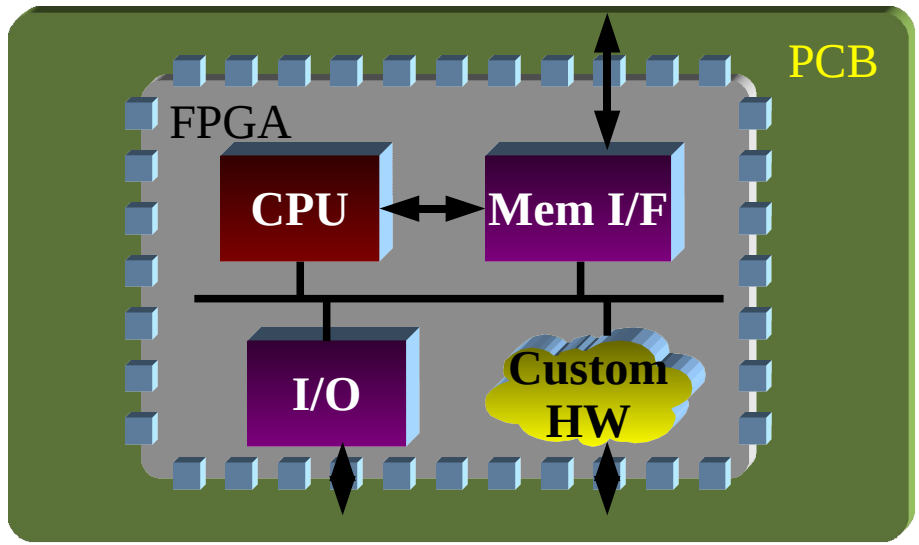
- Processor-centric
  - Embedded Linux subsystem implements core value of the device
  - Linux application may be source or sink for dataflow



Linux on FPGAs – scenarios

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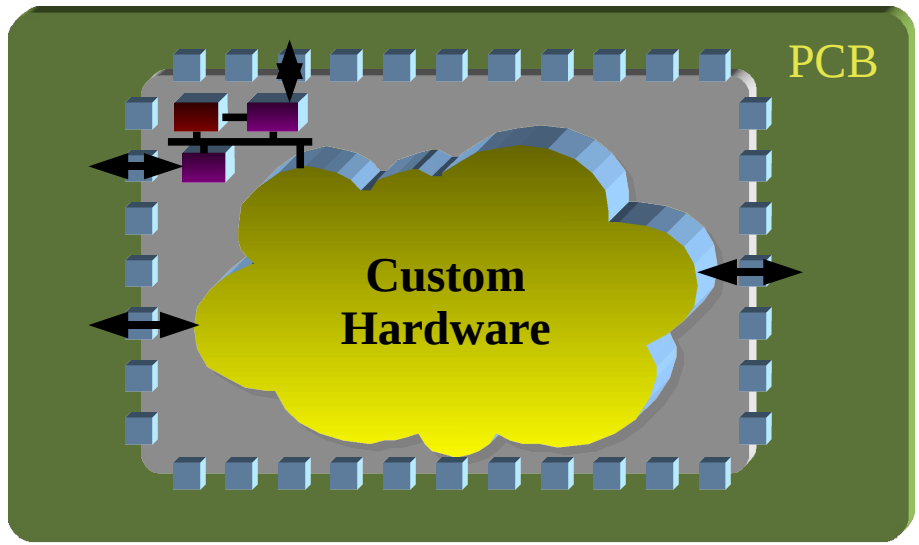
- Logic-centric
  - "conventional" digital subsystem implements core value
  - embedded Linux subsystem sits on the periphery



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Case study – the EBC701

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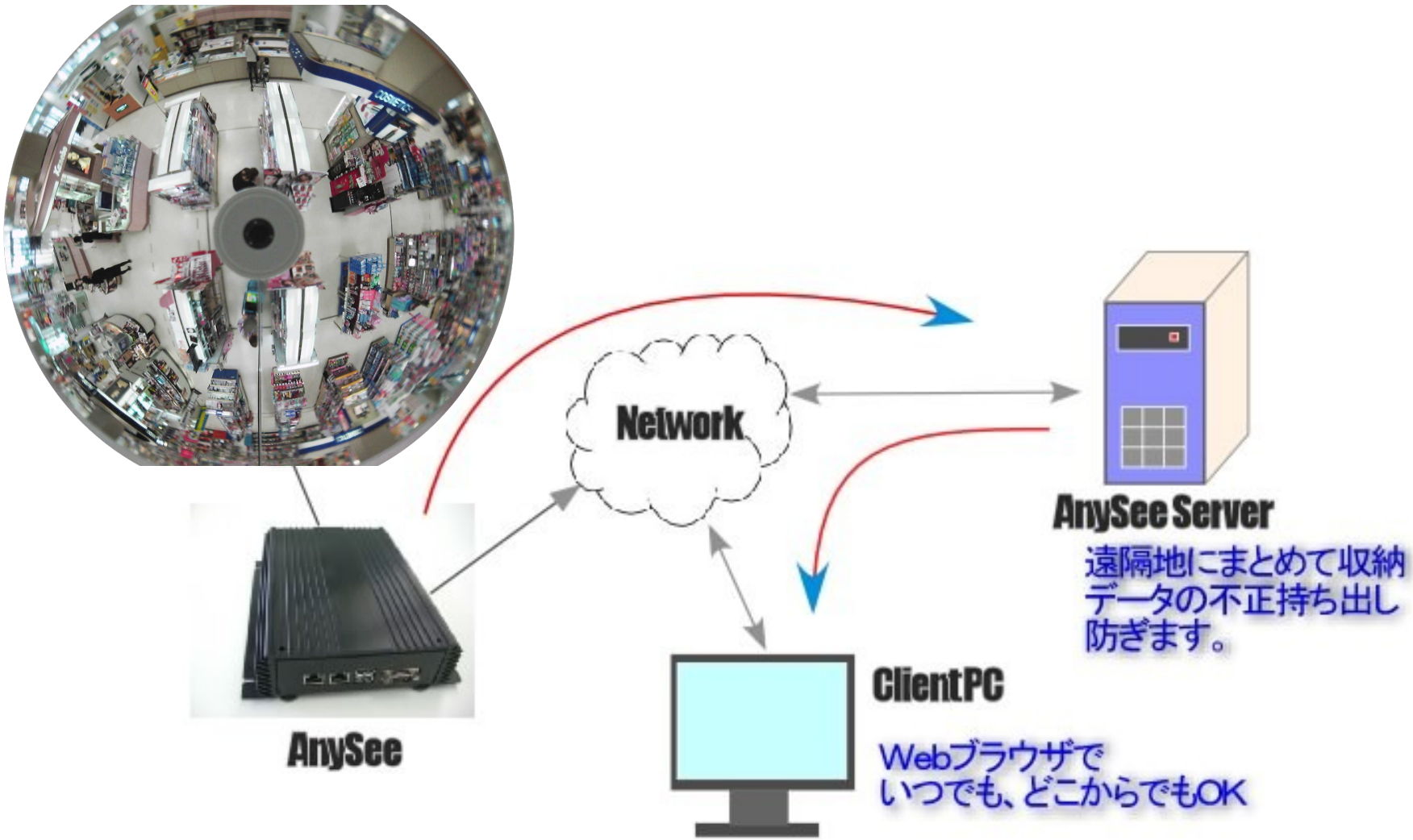
- Intelligent Video application
  - IP camera live JPG stream (1632x1420 @ 4fps)
  - image stream processed by EBC701 FPGA / DAP
    - decode JPG
    - detect and track people in image
  - report image analysis results to central server
- Not surveillance / security
  - Initial application is retail marketing analysis
    - which parts of the shop are busiest?
    - which attract no customers?

Case study – the EBC701



Case study – the EBC701

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- Large Xilinx Virtex5-LXT FPGA with
  - IPFlex DAP DNA2
    - coarse-grained reconfigurable image processing engine
  - dual gigabit ethernet
  - 2x512MB DDR2
  - 32MByte NOR FLASH
  - PCI33 bus
  - Cypress EZUSB Host
  - RS232, misc I/O, debug

Case Study – the EBC701

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- Initial client meeting December 2007
- Initial objectives
  - Boot Linux on EBC701 prototype board
  - Acquire/port gigabit ethernet drivers
- As the customer grew to trust us
  - Integrate 3rd party JPEG decoder IP
  - Management of entire in-FPGA digital subsystem
  - Develop application code
- In the end
  - All in-FPGA HW and SW design and delivery

EBC701 - Project phases

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- Platform
  - Board bringup, support for core infrastructure
    - ethernet
    - PCI
- Functional prototyping
  - Wrapping commercial JPG decoder IP core, interfacing to CPU
  - Interfacing to DAP DirectIO DMA channel
    - Custom FIFO-like interchip DMA protocol
    - Try doing this without an FPGA - bitbang GPIO?!

EBC701 - Project Phases cont'd

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- Production engineering
  - Performance optimisation
    - Getting the CPU out of the datapath
    - Custom bus bridges
    - Image pipeline hardware
- Release engineering
  - Automated testing
  - Manufacturing images (FPGA configs, system flash images)
  - System configuration guides

Linux technologies

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- UIO driver framework (backported to 2.6.20)
  - Trivial kernel-space drivers with core functionality in userspace
  - Wrote light-weight `libuio` to handle UIO device discovery/binding task
  - Low-level device handling code can be shared between Linux app/library and bare metal / device checkout code

Linux technologies

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- Linux desktop as a software prototyping environment for embedded
  - Specified low-level API for hardware interaction
  - Wrote application software spec and subcontracted development
  - Subcontractors developed simulators and stubbed libraries
  - First (and only) integration meeting had application code running correctly on hardware in 15 minutes

EBC701 - Base architecture

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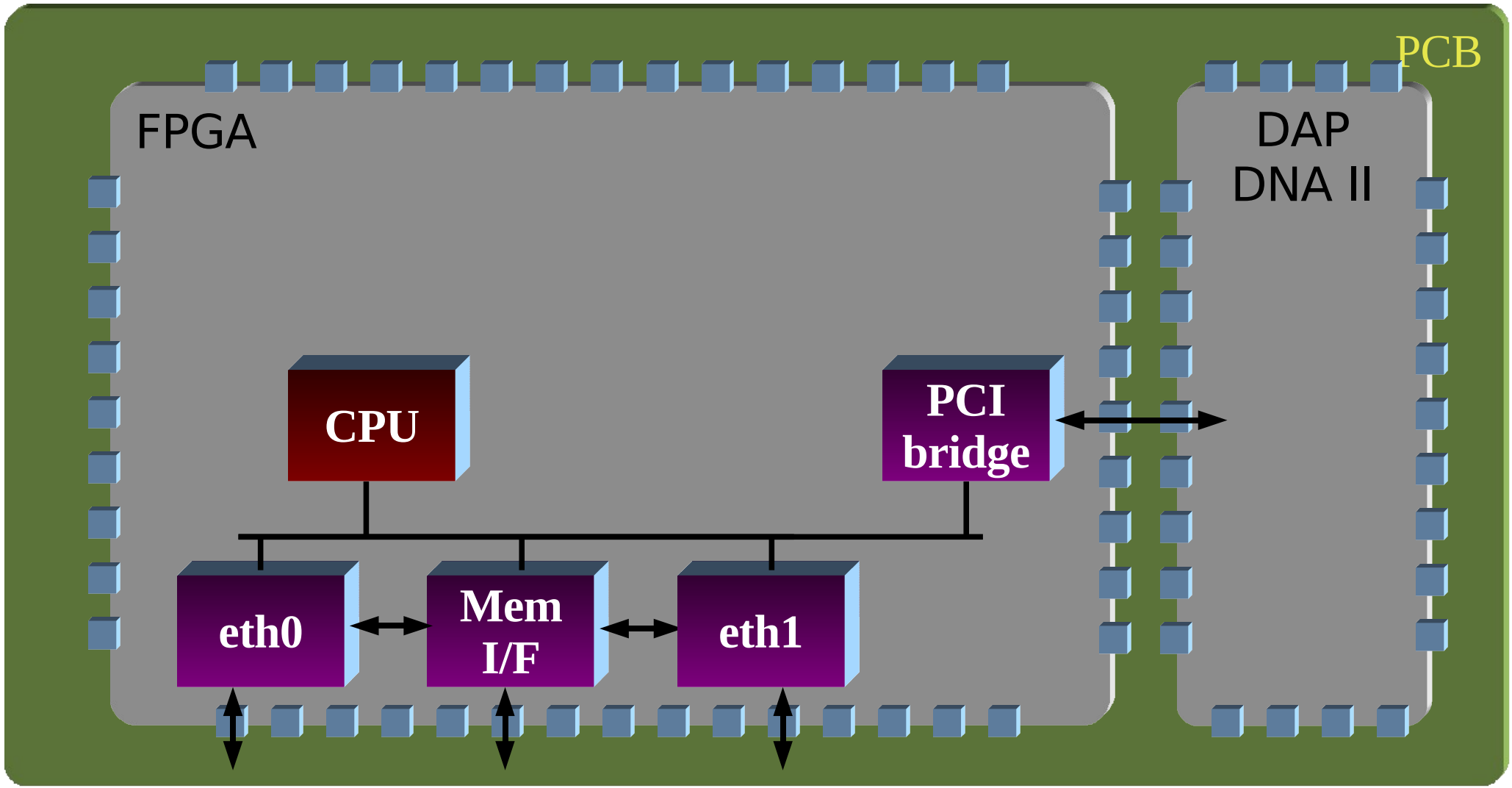

EBC701 - First functional prototype

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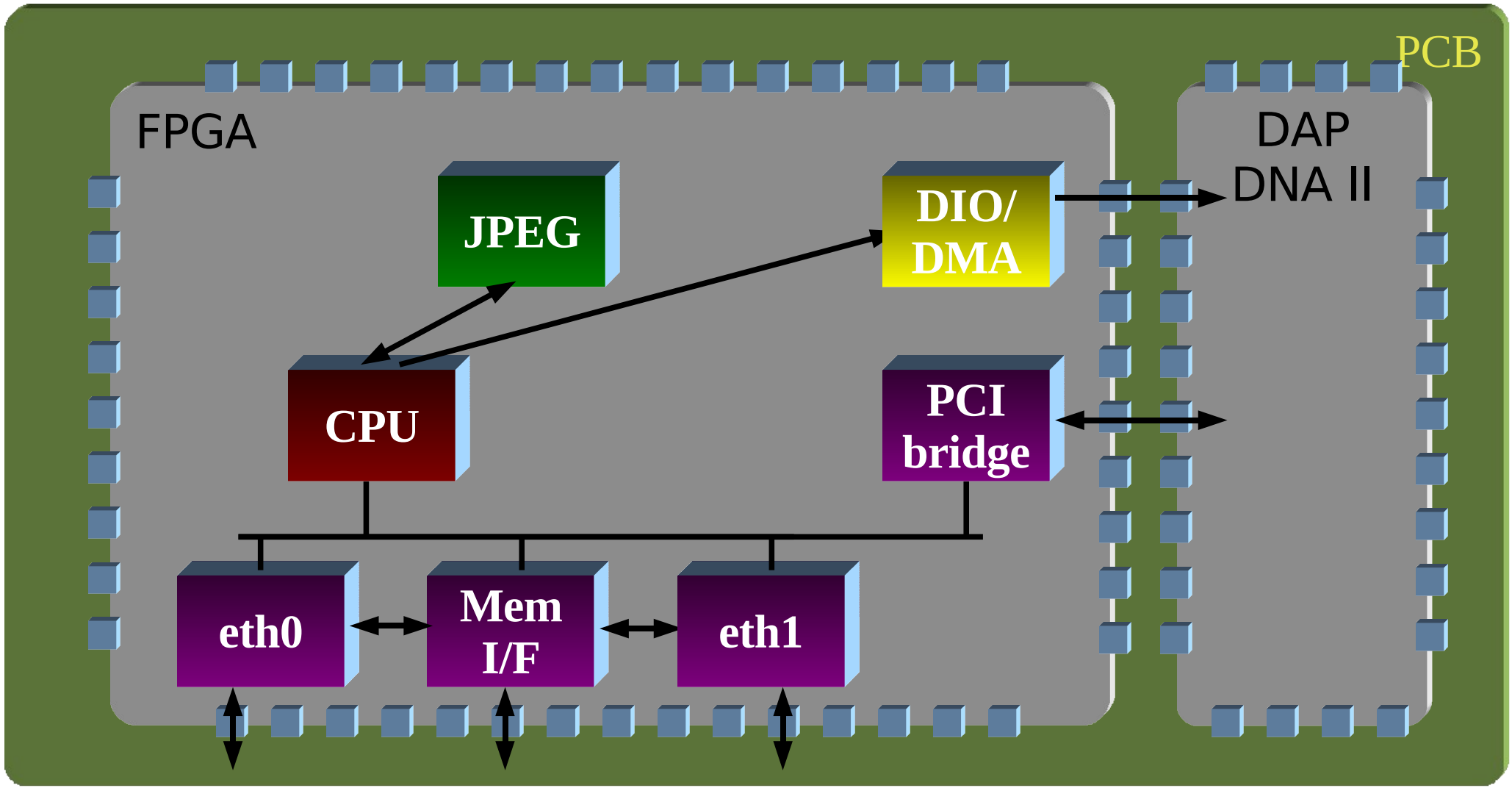

EBC701 – First architecture refactor

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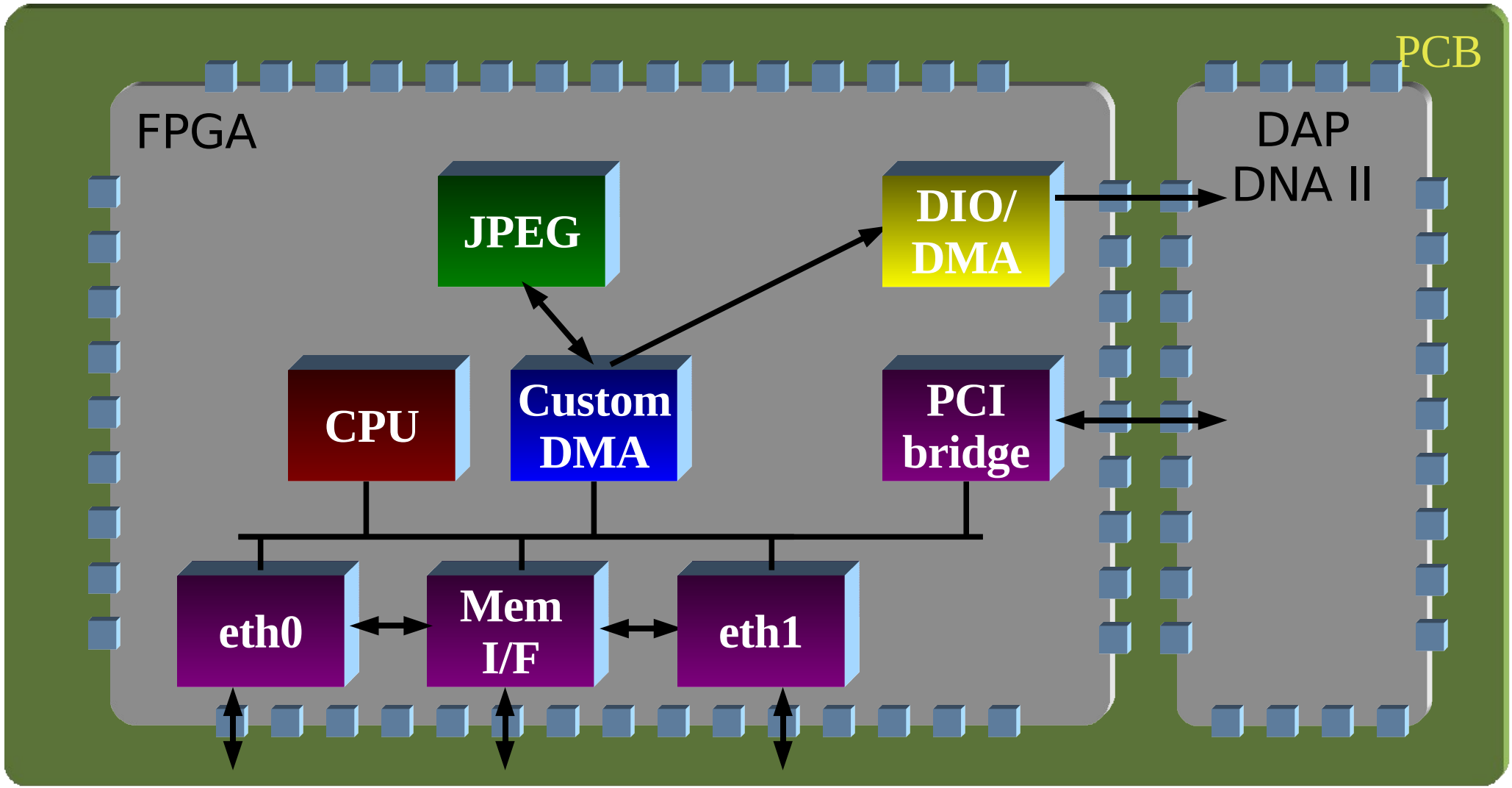

EBC701 – Final architecture

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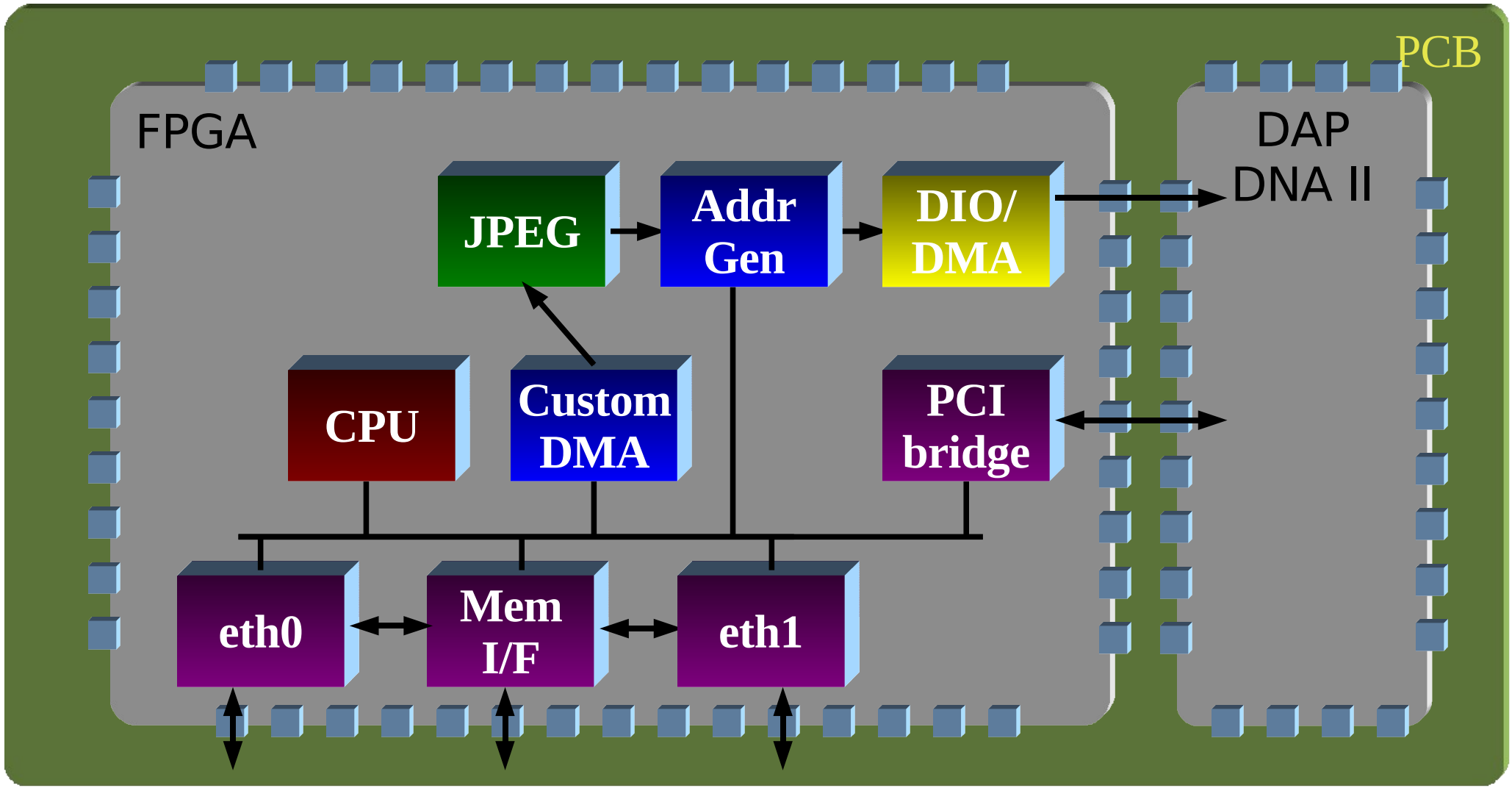

EBC701 – Linux architecture

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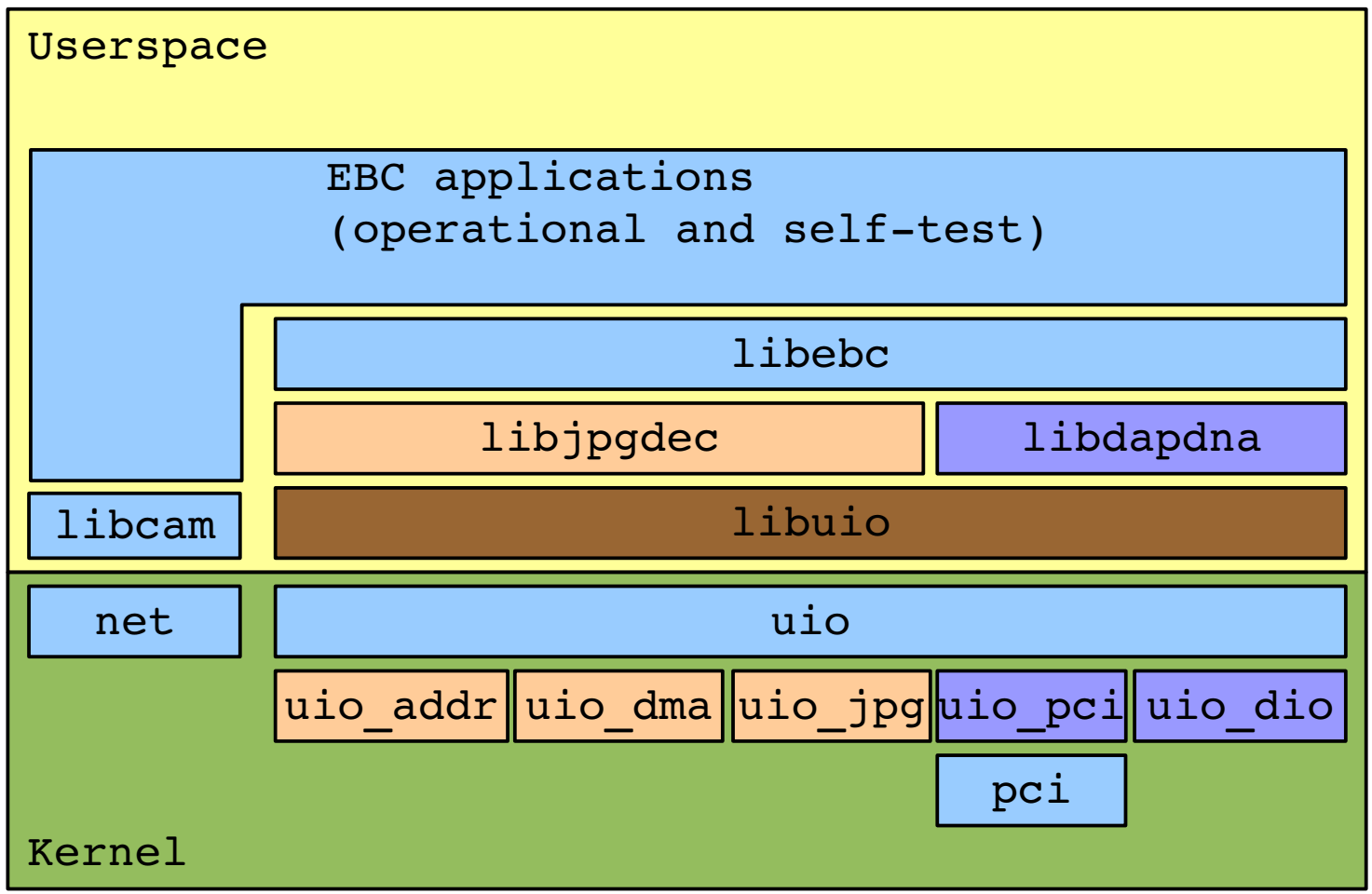
- Build system
  - PetaLinux distribution
    - Customised uClinux-dist plus hardware project support
    - Source-based kernel + libs + standard apps
    - Rootfs generation tools
    - Custom flash image builder tools
- Driver architecture
  - UIO devices for each major HW subsystem
  - Userspace libraries with device APIs around uio interfaces
  - Reused by application and POST and factory test

System software architecture



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Linux on MicroBlaze - timeline

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- Previously
  - 2001/02 Original uClinux-2.4.x kernel port
    - community mailing list established, over 500 members today
  - 2005 PetaLogix formed
  - 2007 - 2.6.20 port from PetaLogix
  - 2008
    - MMU support
    - Flat Device Tree support
    - (aborted) attempt at mainline merge

Linux on MicroBlaze – upstream

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- Xilinx supporting PetaLogix to push MicroBlaze (MMU and noMMU) to mainline
  - Michal Simek doing the hard work for PetaLogix
  - Going for upstream merge 2.6.30 (noMMU first, then MMU)
- Good feedback on LMKL
  - Tom Gleixner steered us to generic timer and IRQ implementation
  - Ingo Molnar likes it:
    - “A quick look at the technical details suggest that arch/microblaze certainly looks like a nicely done architecture.”
    - “It is spartan but uses modern core kernel facilities for everything - genirq, clockevents, generic-time, etc.”

Linux on MicroBlaze - looking forward

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- One challenge with Linux on FPGAs
  - an infinite number of possible hardware platforms
  - traditional BSP concept does not work
- Original solution
  - export a Kconfig fragment from SoC design tools
    - complete description of every system component
    - statically available at kernel compile time
  - Very “static”
    - kernel image is tied to a specific FPGA configuration

Linux on MicroBlaze - looking forward

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- Device trees – a better way
  - textual representation of the system architecture
    - processors, devices, memory, buses, ...
    - IRQs, address ranges, ...
  - DTS compiled into binary blob (DTB) passed to bootloader and kernel
  - automatically populate `platform_device` descriptors, ready for runtime binding to drivers
- DTS adopted for MicroBlaze
  - Auto-generated by a plugin to System-on-Chip design tools – MicroBlaze is first

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Getting involved

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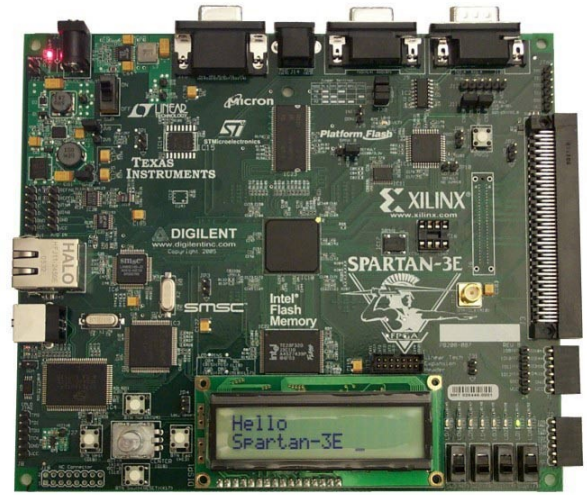
- It's easy to play
  - Xilinx Spartan3E500 starter kit
  - Free/eval Xilinx tools
  - Free PetaLinux distribution
    - http://developer.petalogix.com
    - linux-2.6.20
  - Using latest 2.6.29 kernel requires a bit of roll-your-own for now



Lessons learned

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- General
  - Read the data sheets and errata
    - Then read them again!
- Business
  - When you find a good subcontractor, be nice to them and keep them busy
  - When things are quiet, consider developing things you know your client will want in the future
  - Focus on letting people do what they are best at

Lessons learned

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- Technical
  - Keep the CPU out of the datapath
  - Keep refactoring your code
  - For the right projects, and with the right support (us!), FPGAs + Linux are a killer combination
- `kernel.org` (and upstream generally)
  - merge early, merge often!
  - the longer you wait, the harder it gets

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Backup material

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- DTS Fragment
- ARM comes to FPGAs (Cortex-M1)
- FSL bus and coprocessor connections

DTS fragment

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```
/dts-v1/;
/ {
        #address-cells = <1>;
        #size-cells = <1>;
        compatible = "xlnx,microblaze";
        model = "testing";
        DDR2_SDRAM: memory@90000000 {
                device_type = "memory";
                reg = < 0x90000000 0x10000000 >;
        } ;
        chosen {
                bootargs = "console=ttyUL0,115200 root=/dev/ram";
                linux,stdout-path = "/plb@0/serial@84000000";
        } ;
        cpus {
                #address-cells = <1>;
                #cpus = <0x1>;
                #size-cells = <0>;
                microblaze_0: cpu@0 {
                        clock-frequency = <125000000>;
                        compatible = "xlnx,microblaze-7.10.d";
                        d-cache-baseaddr = <0x90000000>;
```

ARM comes to FPGAs

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- Cortex-M1
  - arm-v6m profile
  - Thumb2-only
    - No ARM instructions at all
  - First FPGA-oriented ARM CPU
- PetaLogix did core kernel port in 2008
  - Basically a Thumb-only kernel, plus
  - M profile exception/IRQ model (NVIC)
    - Shared with arm-v7m – Cortex M3 (silicon IP)
  - `developer.petalogix.com/linux-2.6.x-cortex-m1.git`

Connecting coprocessors to MicroBlaze

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- FSL – Fast Simplex Links
  - Hardware FIFO channels
  - Direct CPU connection
    - Up to 16 in each direction
  - Single cycle read/write to/from register
  - Intended as custom coprocessor interface
- Problem
  - CPU in the datapath!
- Great for fine-grained coprocessors
- Not so good for big data processing