

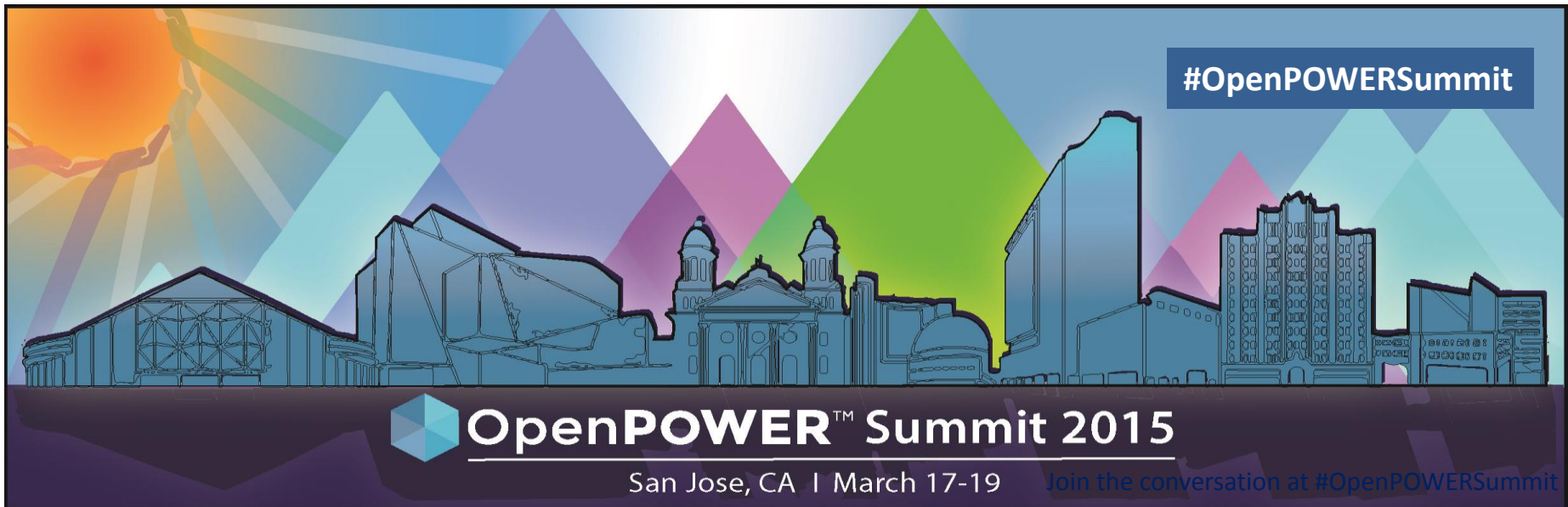


# Data Center and Cloud Computing Market Landscape and Challenges

**Manoj Roge,**

Director – Wired & Data Center Solutions

Xilinx Inc.



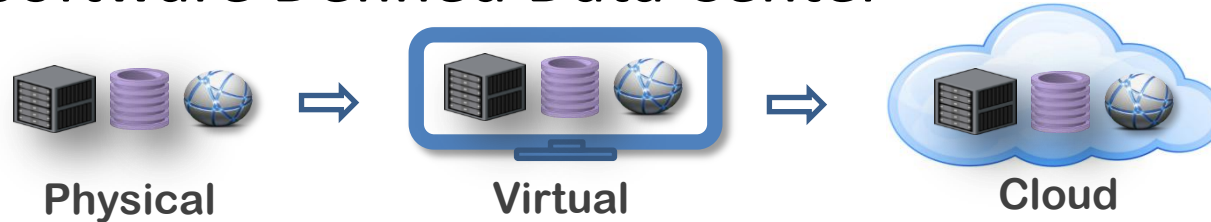
# Outline

---

- Data Center Trends
- Technology Challenges
- Solution Options
- Xilinx Focus
- OpenPOWER Developments

# Data Center Trends

- Software Defined Data Center



- Evolving Architectures & Standards



- Need for Workload Acceleration

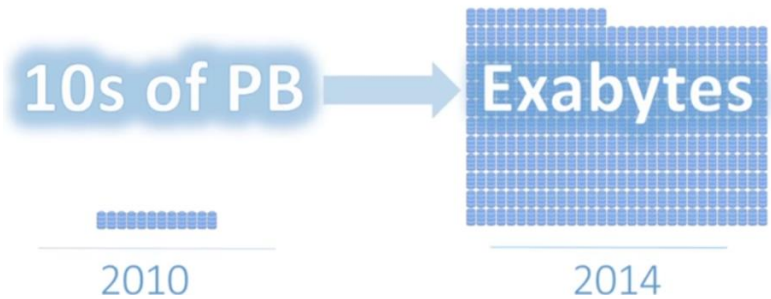


# Exponential Growth

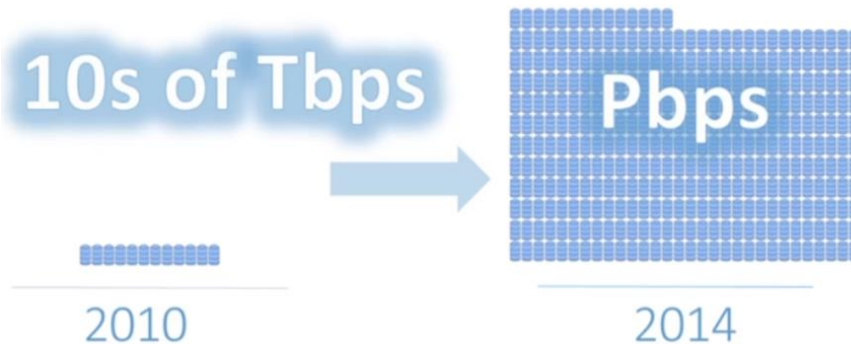
## Compute



## Storage



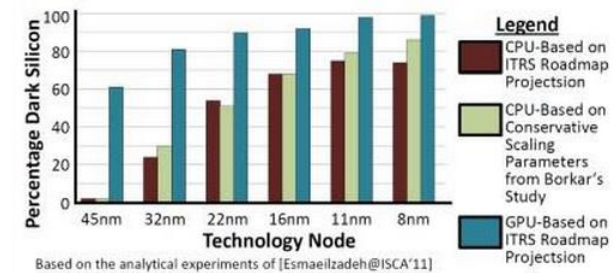
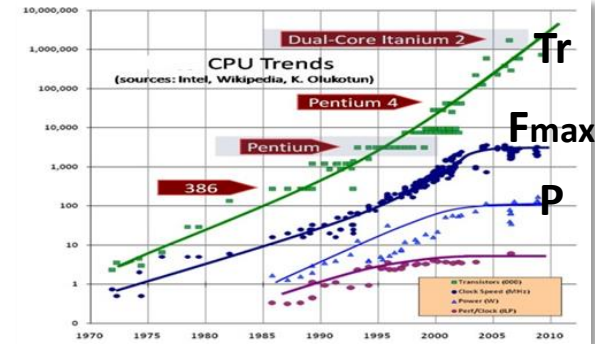
## Network Capacity



Source: ONS2014 Keynote, Microsoft / Azure

# Technology Challenges

- Power/thermal density is limiting Fmax scaling
  - End of Dennard scaling  $\Rightarrow$  End of Moore's law
  
- CPU performance scaling problematic
  - Difficulties in exploiting task-level parallelism with multi-core  $\Rightarrow$  Dark silicon
  
- Heterogeneous computing  $\Rightarrow$  Best of both worlds
  - Higher performance and lower power
  - Increased compute density



# Need for New Data Center Architecture

---

- Think beyond traditional architecture
  - Need scalable architecture to boost system performance & reduce latency
- Design for application acceleration & processor offload
  - Heterogeneous processing for specialized workloads
- Need to improve customer CAPEX and OPEX
  - Performance/Watt must be key consideration

# How can FPGAs help Acceleration?

## COMPUTE

Image Search  
8x throughput

Video Transcode  
20x throughput

Image Processing  
50x throughput

## STORAGE

Hybrid memory  
Latency hiding  
10x power saving

Key-Value Stores  
36x RPS/Watt  
10x-100x latency reduction

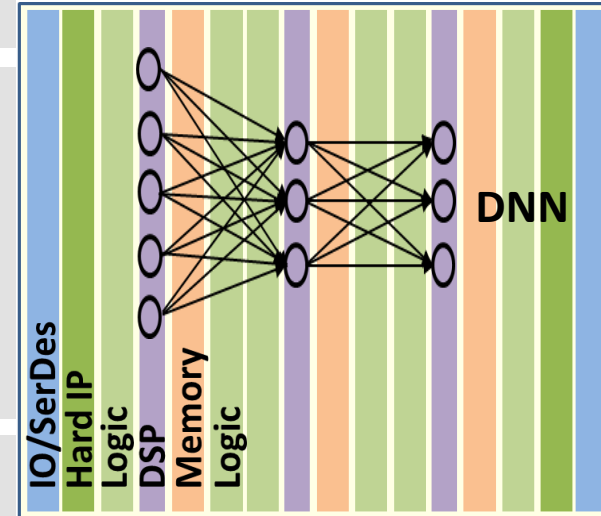
Compression/Encryption  
Customize algorithms  
Latency sub 5us  
Encryption rate 10x

## NETWORKING

Secure socket  
Latency sub 5us  
Encryption rate 10x

TCP endpoint  
Latency sub 2us  
10x virtual circuits

Packet switch  
Latency sub 100ns  
Protocol choices



FPGA Architecture  
(Conceptual)

# Barriers to Adoption: Ease of Programming

## Need

## Solution Attributes

**High Performance / Watt**

### Architecturally Optimizing Compilation

- Compiler needs to be fast and efficiently utilize resources
- Can develop accelerators with high performance/watt

**Complete SW Development Environment**

### Software Development Flow for FPGA Hardware

- Single Environment for software workflows
- CPU/GPU like development environment

**Easily Upgradeable**

### Reconfigurable Optimized Accelerators

- Need accelerator flexibility for different applications
- Require always on IO and networking interfaces

**Xilinx Has Complete Hardware and Software Solutions**

Join the conversation at #OpenPOWERSummit

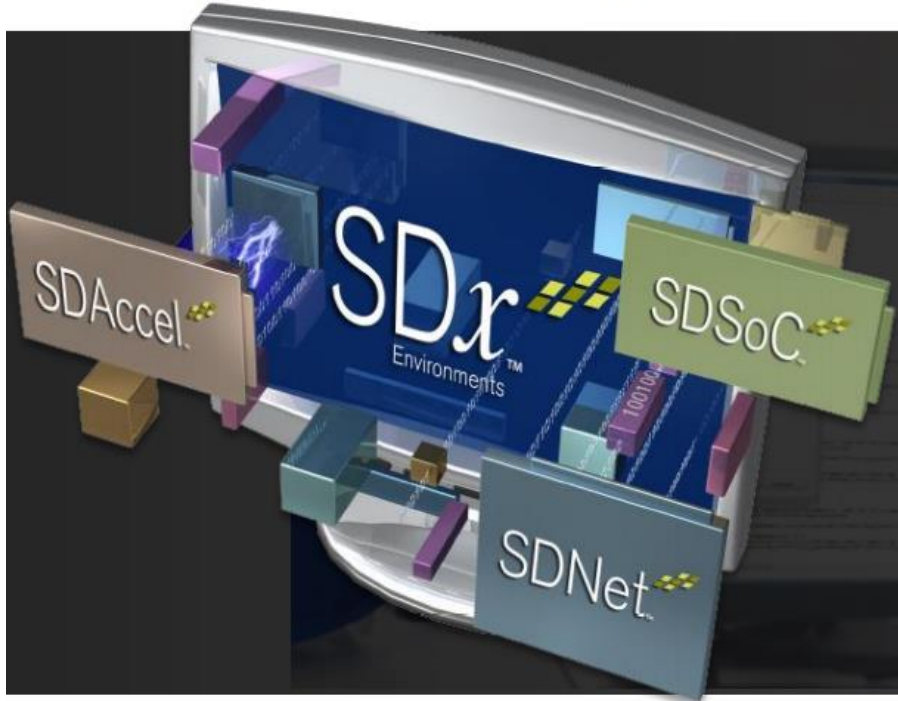


**OpenPOWER™**



# Software Defined Development Environments

C, C++, OpenCL, Domain-specific

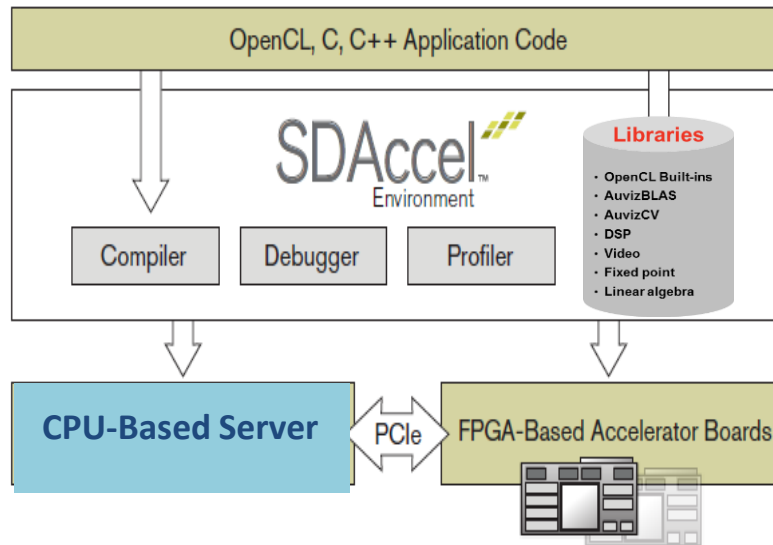


- ✓ SDAccel for OpenCL, C, C++ enables up to 25x better performance per watt
- ✓ SDSoC provides greatly simplified ASSP-like C, C++ programming experience
- ✓ SDNet allows creation of 'Softly Defined Networks'

**Expand Users to Broad Community of Software and Systems Engineers**

# First Complete CPU/GPU Development Experience on FPGAs

*Only FPGA Vendor with C, C++, OpenCL*



SDAccel<sup>™</sup>  
Environment

## CPU/GPU-Like Development Experience

- ✓ Complete software workflow for developers with little to no prior FPGA experience
- ✓ CPU emulation, co-simulation and native hardware
- ✓ Automatic instrumentation of compiled accelerators with profiling visibility across host and kernels

Leverage Existing C & C++ Code Base

# OpenPOWER and Xilinx Driving Heterogeneous Computing

---

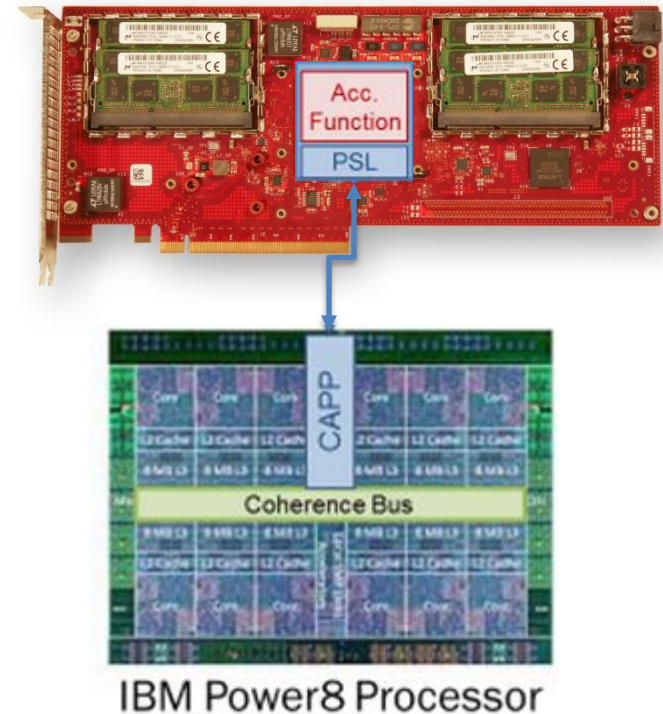


- Open Innovation required to innovate across full HW & SW stack
  - OpenPOWER has setup impressive ecosystem for collaboration
- FPGAs are a natural fit in rapidly evolving markets
  - Parallel architecture, flexibility and configurability are its strengths
- Power8 + FPGA with CAPI (Coherent Accelerator Processor Interface)
  - Custom acceleration engine on coherent fabric of the POWER8
- CAPI removes overhead & complexity of IO subsystem
  - Allows FPGA accelerator to operate as part of an application

# Convey CAPI Developer Kit for Xilinx FPGAs

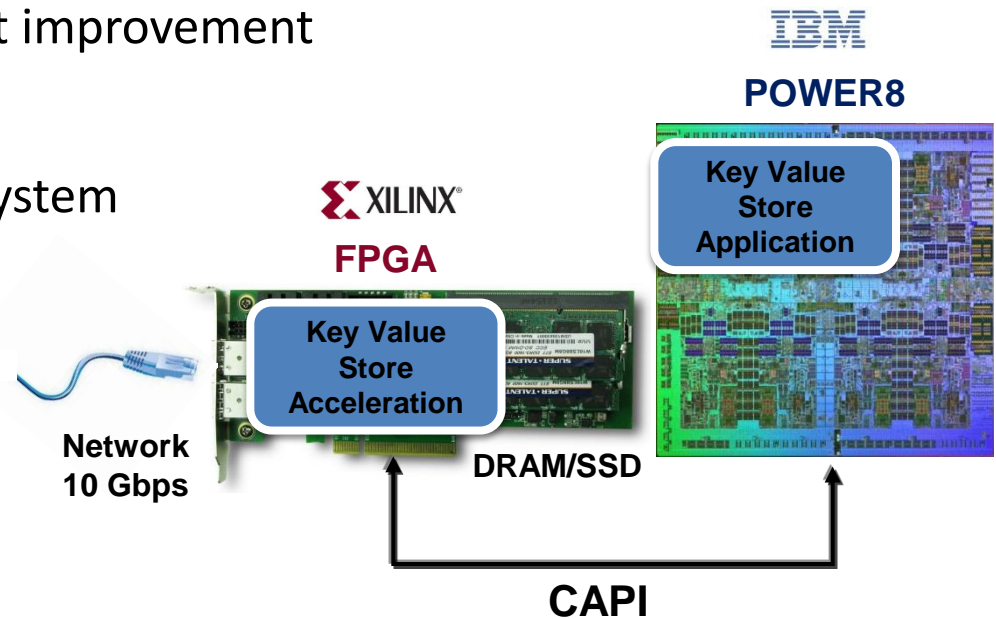
- CAPI Developer Kit enables application specific acceleration on IBM Power 8 systems
- Convey's Eagle coprocessor delivers high density FPGA acceleration and large, high bandwidth on-board memory in a PCIe form factor
- Xilinx XC7VX980T FPGA provides capacity and bandwidth for complex, highly parallel designs

## Convey-Xilinx Accelerator



# Xilinx Key-Value-Store with CAPI

- Power8 + FPGA connectivity with CAPI
  - Enables seamless application acceleration
- Acceleration
  - 35x performance per watt improvement
- 10x latency reduction
  - Enables hybrid memory system
- Combines DRAM & SSD
  - Integration with OpenCL



# Summary

---

- Rethink data center architecture to address scaling
- Need for workload acceleration – FPGA acceptance
- SDAccel offers CPU/GPU development experience on FPGAs
- Xilinx demonstrating CAPI-based acceleration solutions
- Excited to drive Innovation through OpenPOWER
- Visit Xilinx Booth #913

Follow Xilinx on:



[facebook.com/XilinxInc](https://facebook.com/XilinxInc)



[twitter.com/XilinxInc](https://twitter.com/XilinxInc)



[youtube.com/XilinxInc](https://youtube.com/XilinxInc)

# Q&A

