



# **An Open Architecture, Server-Based Solution for Next Generation Electronic Warfare System**

**19 March 2015**

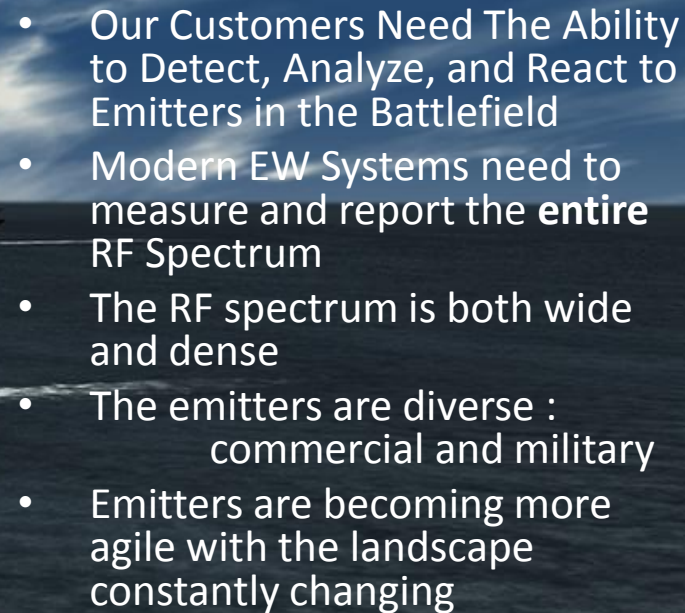
**Greg Gannett**



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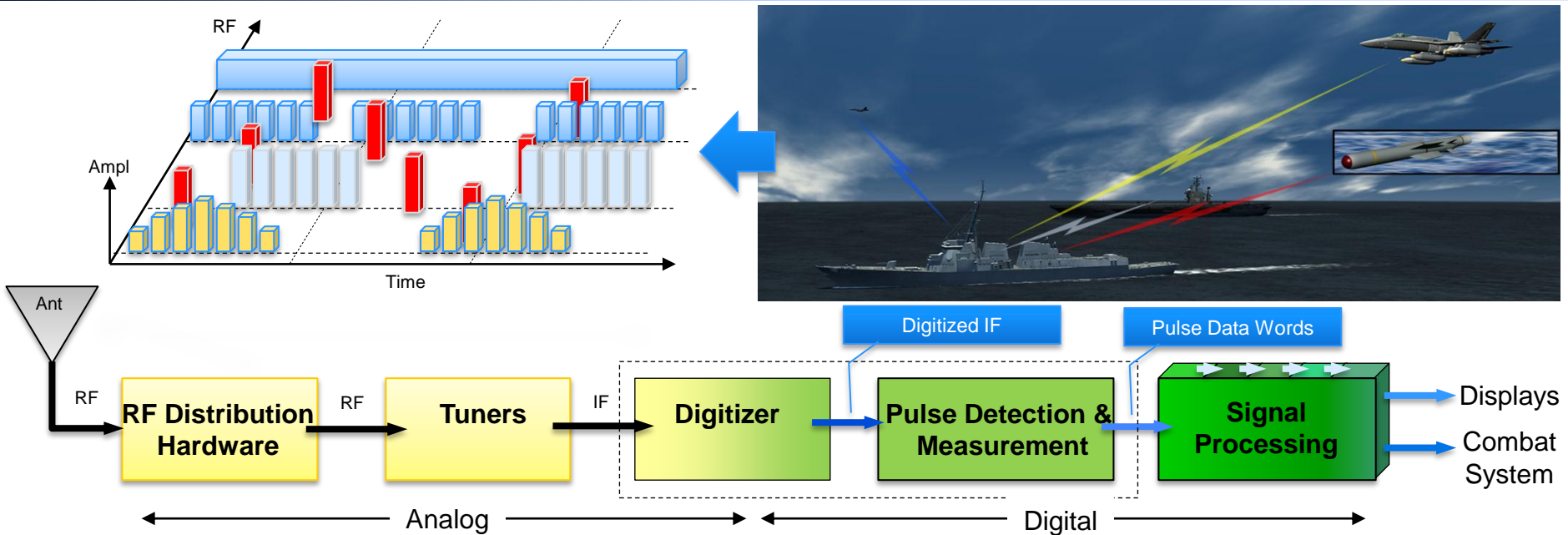


- **Electronic Warfare Overview**
- **IR&D Backstory**
- **System Architecture**
- **Network and GPU Performance**

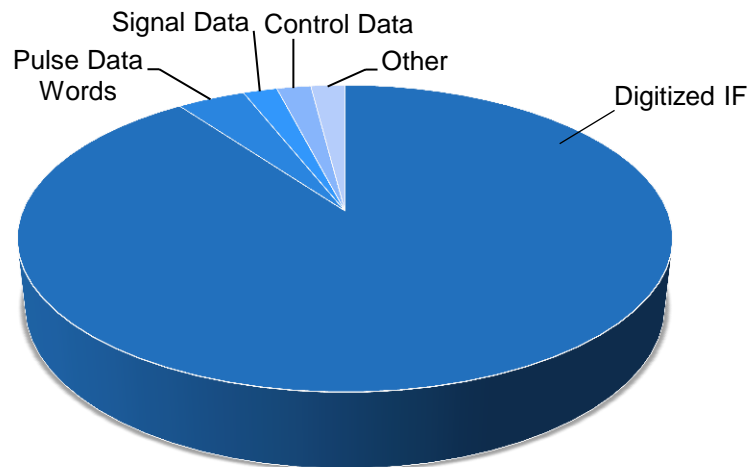


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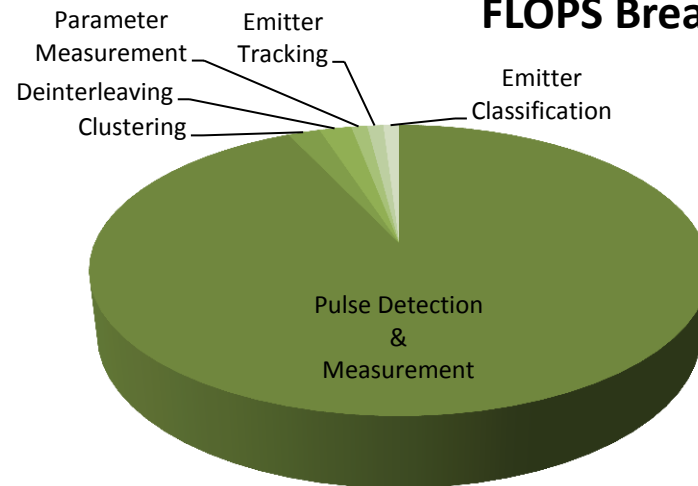
# EW System Architecture - Basic



## IO Bandwidth Breakdown



## FLOPS Breakdown

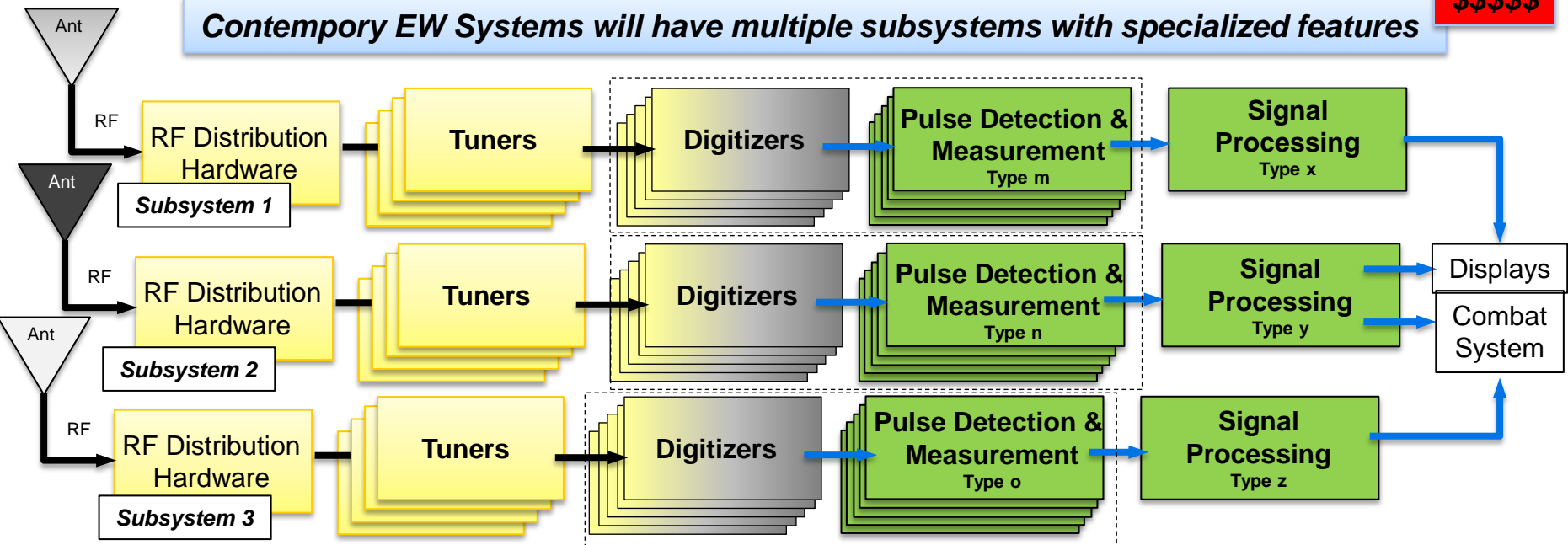


# EW System Architecture – Scaled



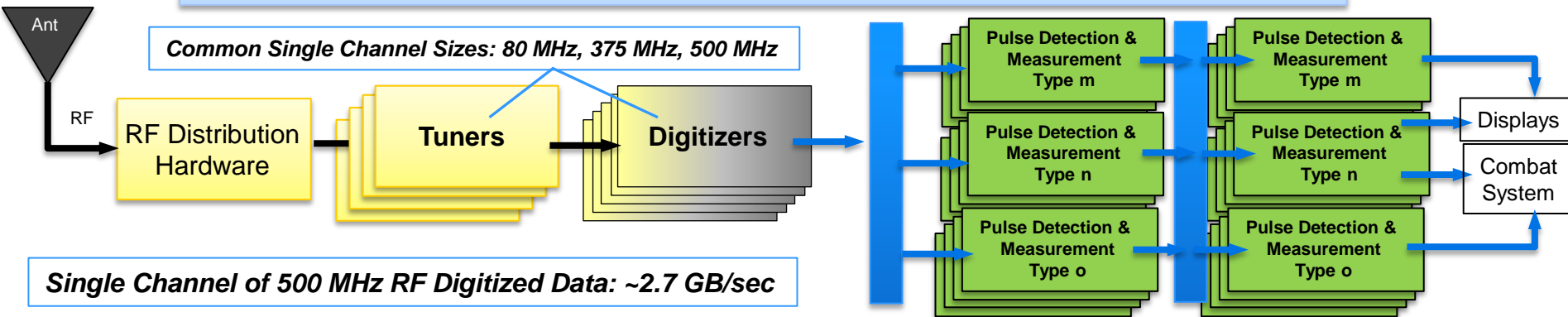
**Contemporary EW Systems will have multiple subsystems with specialized features**

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**Alternative: Digitize Once, Publish CDIF Data to Pulse and Signal Processing**

\$





## ■ Key Tenants Envisioned for Next Generation EW System Architectures

- Digitize the Spectrum and Distribute CDIF via a Flexible Digital Backbone
- Deliver new capability via mission and target-specific software applications hosted on a common hardware solution
- Replace custom, proprietary interfaces with open, standardized interfaces to facilitate rapid and affordable capability insertion

## ■ Server-Based Electronic Warfare Engineering Development Model

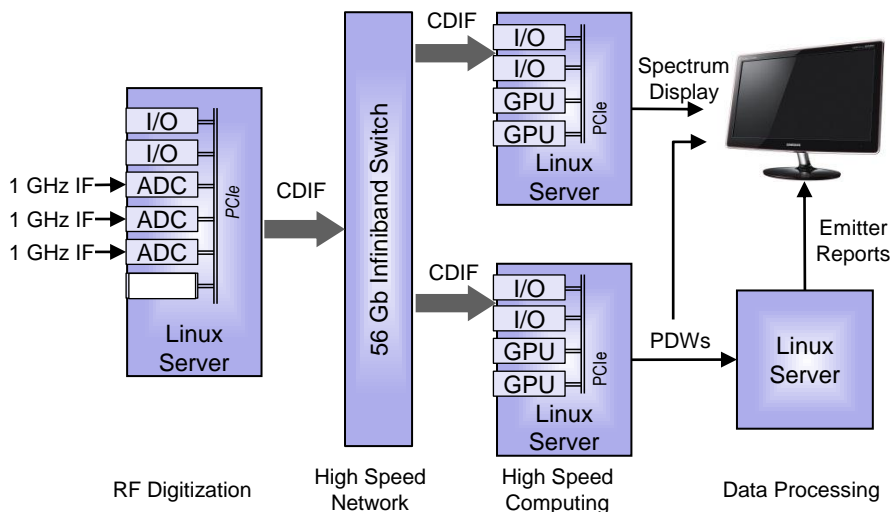
- Objective: To evaluate the ability of current & projected COTS technologies to realize Next Gen EW Architecture Vision

# Server-Based Electronic Warfare Demonstrator

## Advanced Development Model Overview








### Architecture



### Objectives

- ✓ Validate key COTS technologies: RF digitization, high-speed networks and high-speed computing environment
- ✓ Migrate pre-existing FPGA and PowerPC based receiver processing to Linux Servers and Intel & NVIDIA accelerators
- ✓ Demonstrate scalability of architecture to greater bandwidths (wideband feasibility)
- ✓ Validate Open Interface Data Distribution Services (DDS) publish / subscriber services
- ✓ Verify key TPMs: CDIF throughput, Processing Bandwidth, Measurement Accuracy, Dynamic Range

### Enabling Technologies

COTS A/Ds Digitizers	PCIe Gen 3.0	High Speed Network	General Purpose GPUs	Intel Xeon Multicore CPUs
 <ul style="list-style-type: none"> <li>• Easily scaled across general purpose HW hosts</li> <li>• Flexibility in configurations</li> <li>• Publish source I&amp;Q data</li> <li>• <b>Today:</b> 12 bit @ 500 MHz</li> <li>• <b>Next Gen:</b> 16 bit @ 500 MHz</li> </ul>	 <ul style="list-style-type: none"> <li>• Open standard with accelerated performance road map</li> <li>• More configurable, higher bandwidth than VME</li> <li>• <b>Today:</b> 7.88 GB/sec (8xGen 3)</li> <li>• <b>Next Gen:</b> 15.7 GB/sec (8xGen 4)</li> </ul>	 <ul style="list-style-type: none"> <li>• Widely used open standard provides most bandwidth solution</li> <li>• User level multicast</li> <li>• Near term (2015) projection of &gt;100 Gbps</li> <li>• <b>Today:</b> 7GBps per channel</li> <li>• <b>Next Gen:</b> 12.5 GBps per channel</li> </ul>	 <ul style="list-style-type: none"> <li>• Excellent GFLOP/watt ratio</li> <li>• Cost benefit over FPGA</li> <li>• High-order SW language</li> <li>• Vast CUDA libraries</li> <li>• <b>Today:</b> Kepler GPUs with ~5 GFLOPS per watt</li> <li>• <b>Next Gen:</b> Maxwell GPUs with ~12 GFLOPS per watt</li> </ul>	 <ul style="list-style-type: none"> <li>• Excellent GFLOP/watt ratio</li> <li>• Supports numerous High-order programming languages</li> <li>• Most mainstream target processing environment</li> <li>• <b>Today:</b> 2600 Xeons</li> <li>• <b>Next Gen:</b> Xeons with Phi Accelerator</li> </ul>

**100% COTS Architecture Provides an Open, Scalable, Upgradable and Affordable Solution**



# EW Advanced Development Model – First Generation



**Next Generation EW System** – *Tactically Relevant, Multi-Channel, Open Architecture EW Solution*



**Digitization Layer**– *COTS A/D Solution Digitizes and Multicasts all CDIF Data to a Scalable Number of Processing Nodes*



**Processing Layer** – *COTS GPGPUs Perform Bulk of Real-Time Signal Processing with Multi-Core CPU's Completing the Balance*

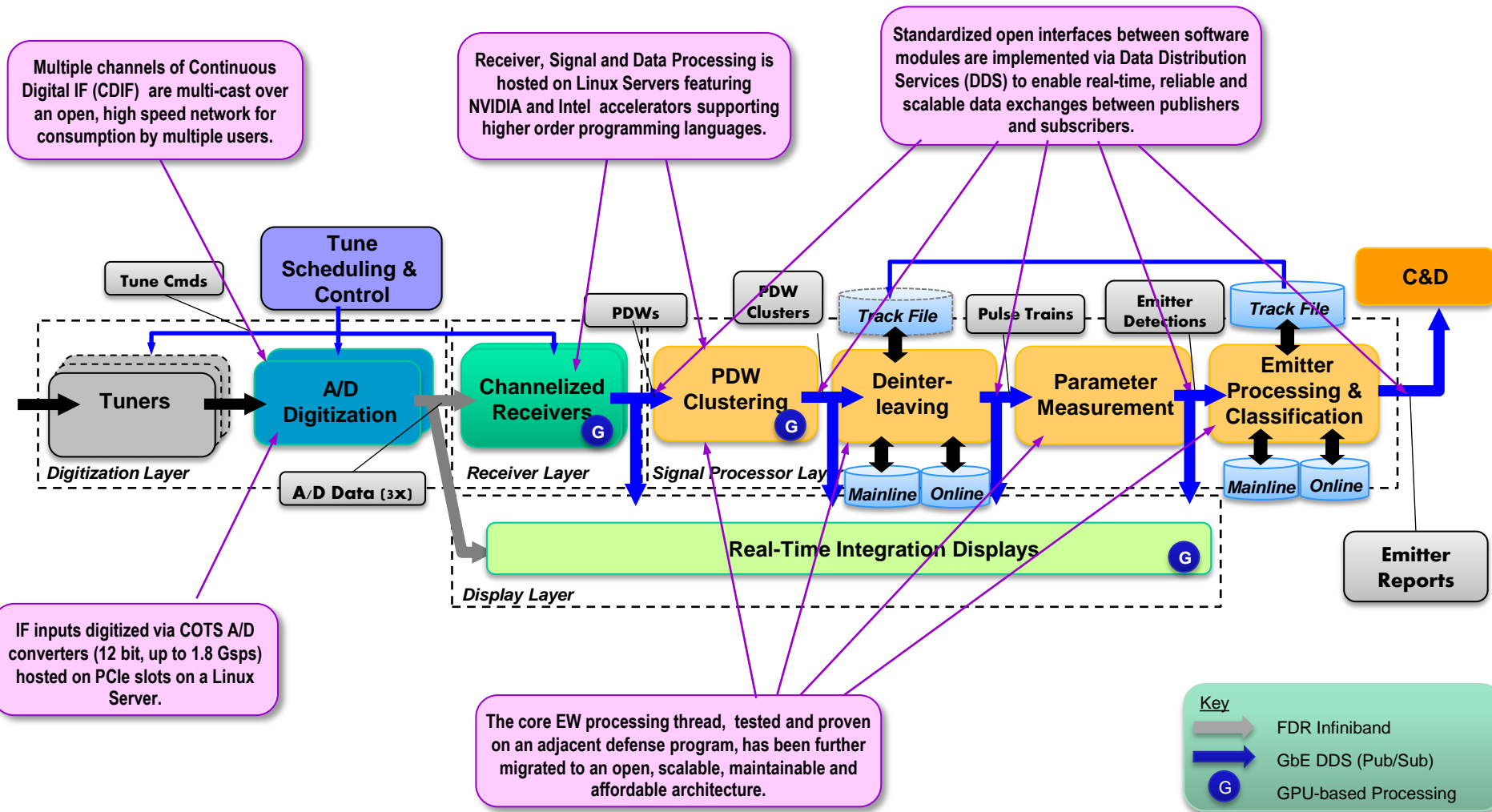


**High Speed Network**– *56 Gbps per channel Infiniband Network*



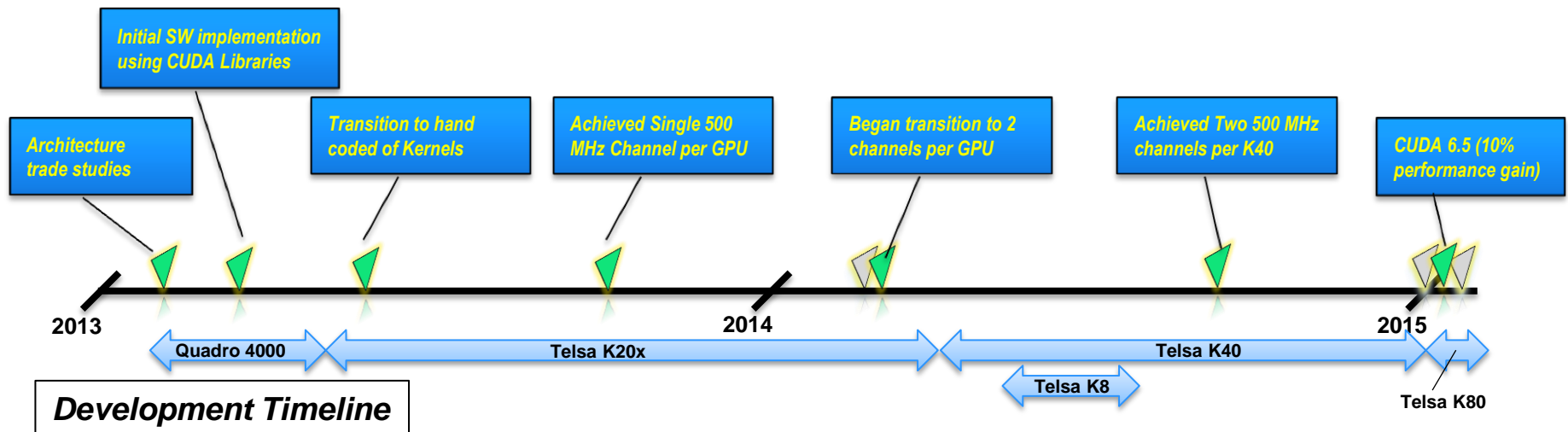
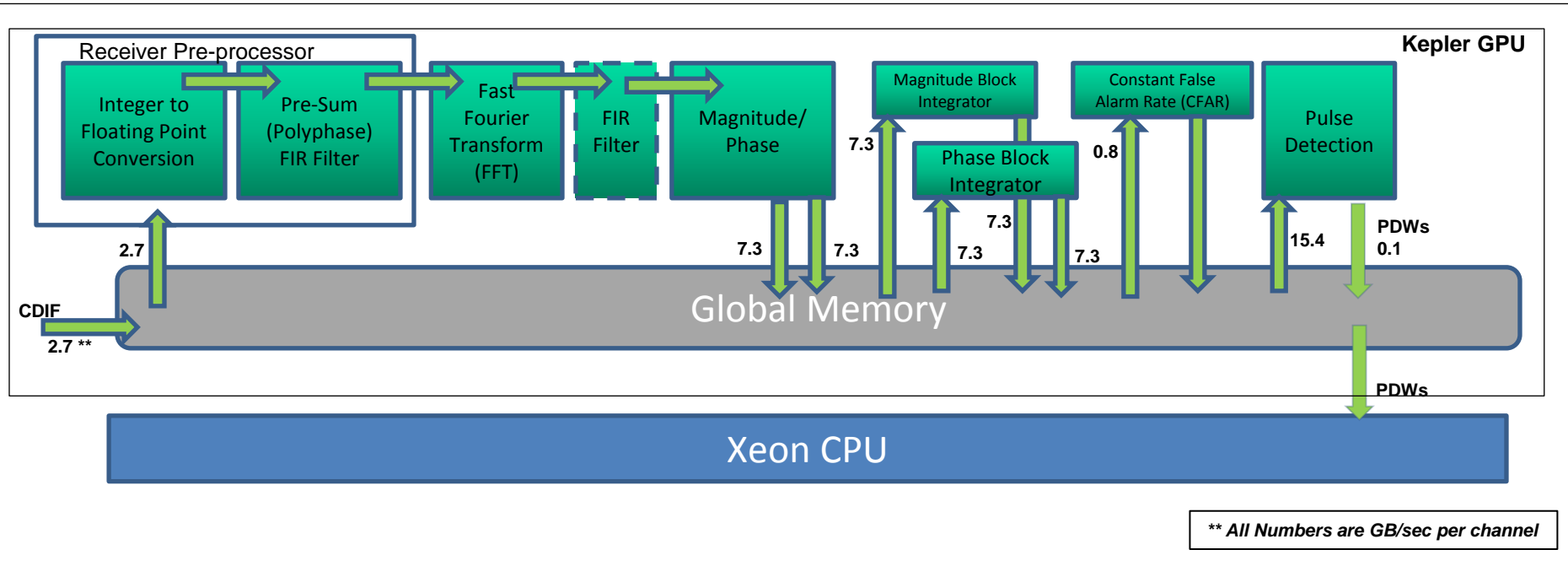
# Server-Based Electronic Warfare ADM

## Software Overview



Open Architecture and Modular, Software-Based Solution Facilitates Rapid Capability Insertion in Response to New and Evolving Threats

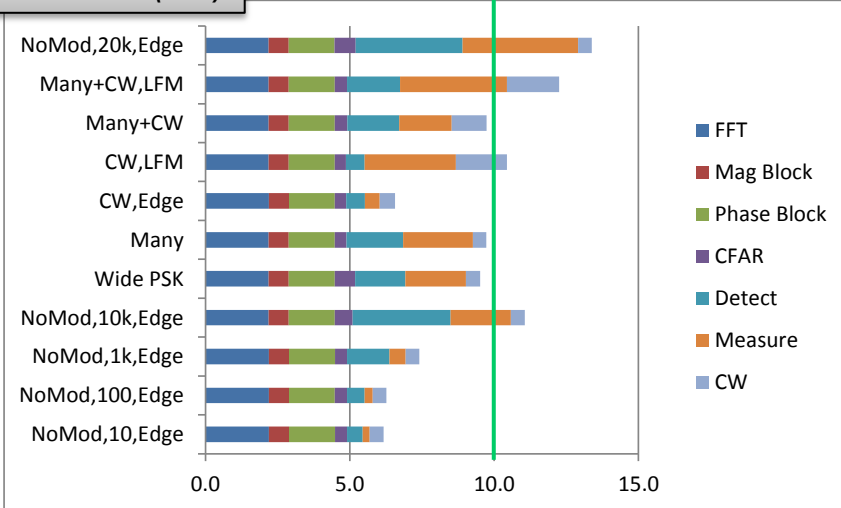
# Channelized Receiver GPU Implementation & Timeline



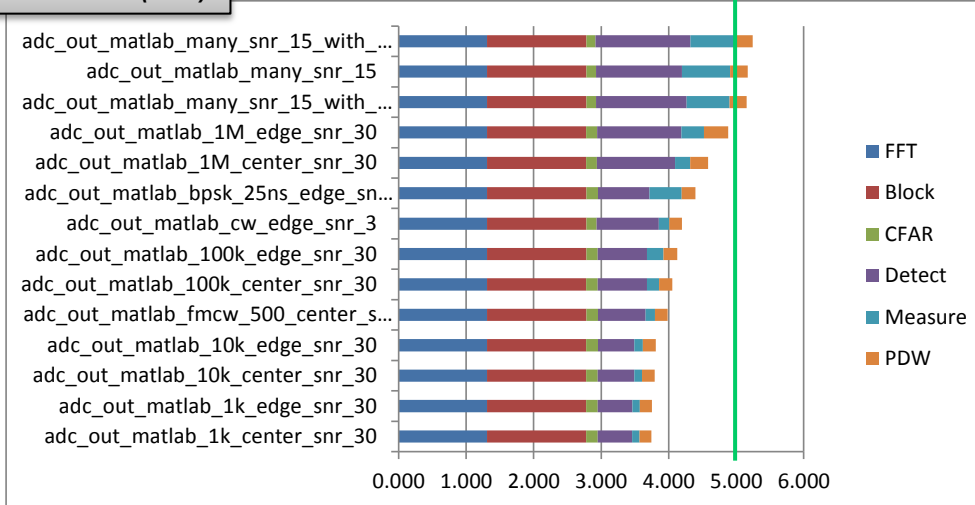
# Benchmarks – 3 Generations of GPGPUs



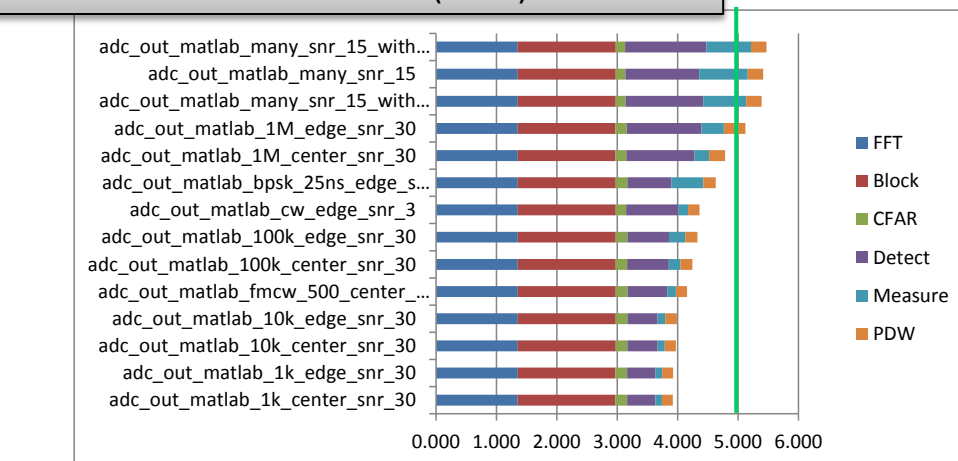
**Tesla K20x (3/14)**



**Tesla K40 (1/15)**



**Tesla K-80 Performance – on one (of two) GK210 GPUs**

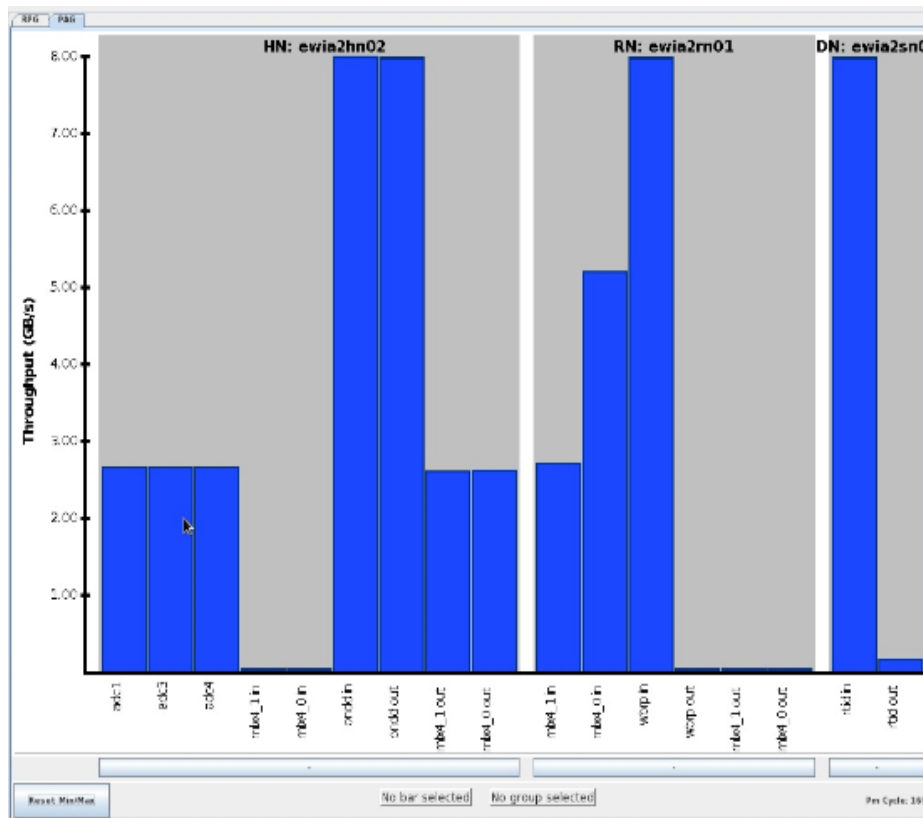


**Tesla K-80 Single Precision Performance (Constant Data Stream)**

Kernel	K40	K80 (per GPU)	
Samples	13330000	13330000	
Threads	1666250	1666250	
Ops	1.14638	1.14638	Gflops
Time	1.058	1.185	ms
Ops/s	1084	967	Gflops

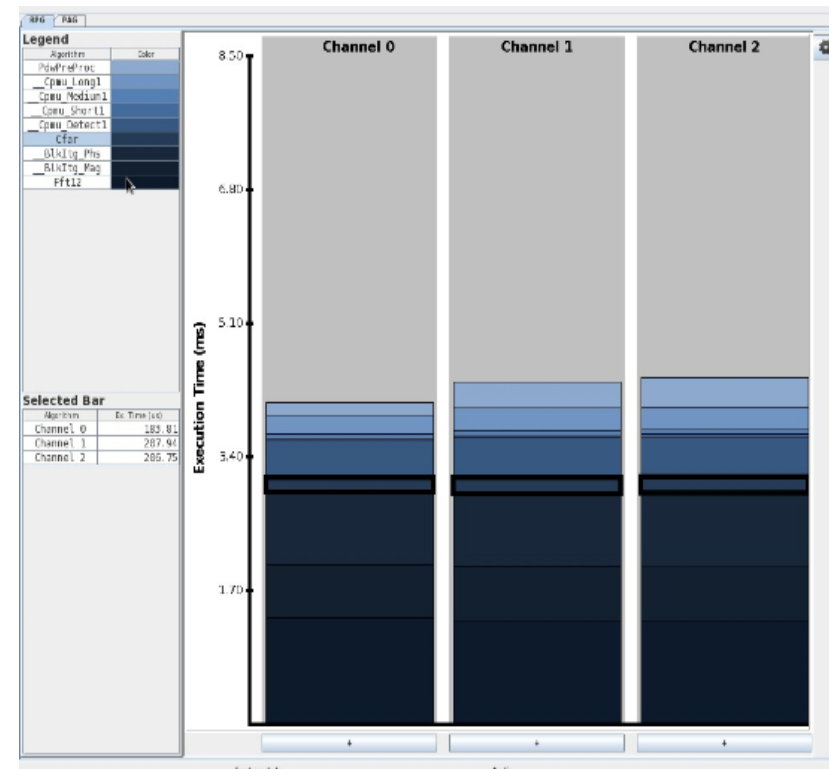
**700 GLOPS typically advertised for Single Precision cuFFT processing (FFT length of 4096)**

cuFFT 6.0 on K40c, ECC ON, 32M elements, input and output data on device

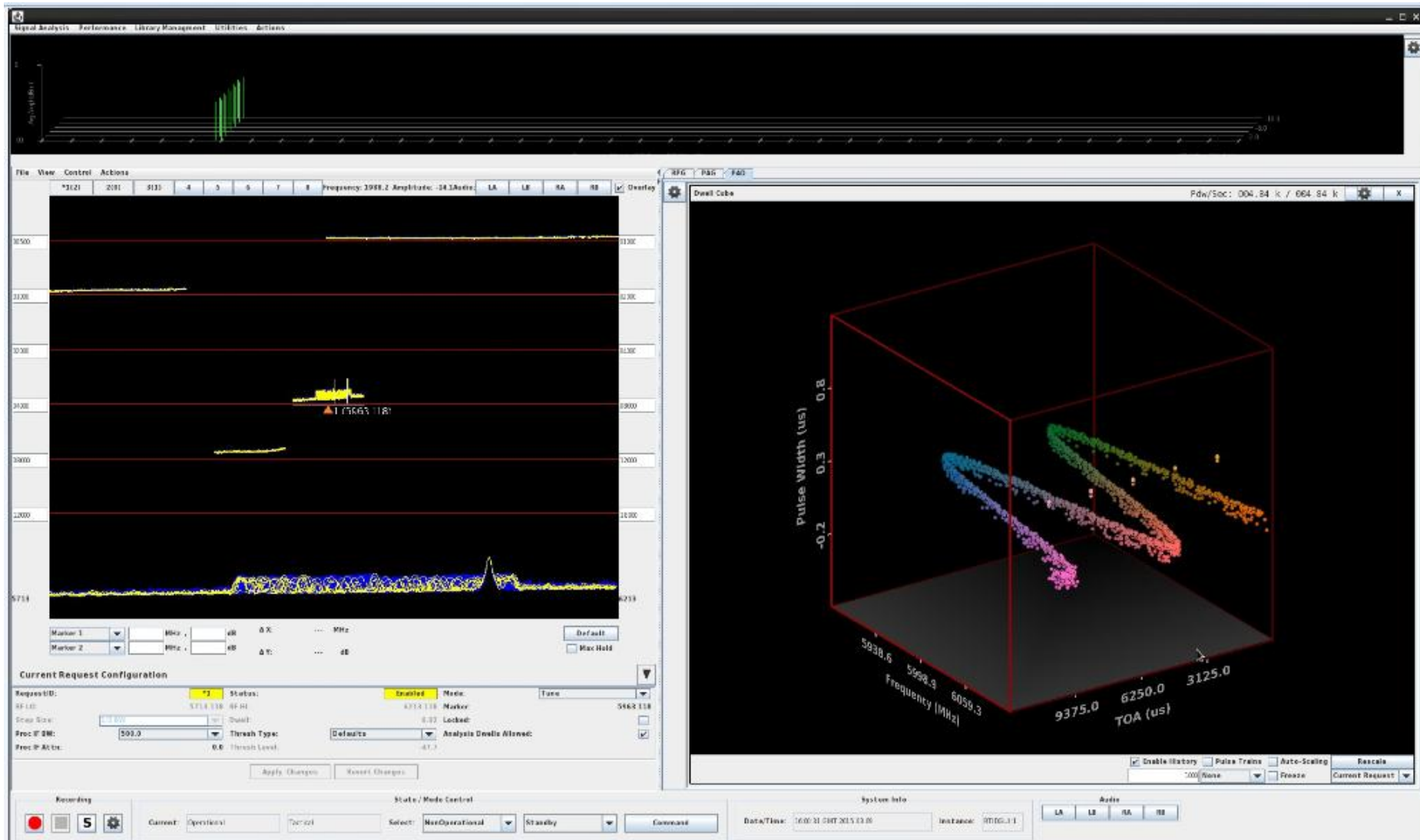


- Software monitors utilization of GPU resources
- Color-codes various stages of the Channelized Receiver processing over time

- Software monitors all network related resources and provides real-time feedback on current throughput
- Screen capture confirms Multicast Infiniband of high bandwidth Digitization Data



# Signal Processing Displays



**Both Core Signal Processing Software and Real-time Signal Processing displays hosted on GPU processors**



## ■ Conclusions

- The Enabling Technologies are moving fast driven by wide commercial / non-defense markets
- We continue to be encouraged by results to date and anticipate continued performance gains due to ongoing COTS evolution

## ■ Next Steps

- The transition of this server-based architecture to a tactical system is underway
- Extend architecture to additional applications across the RF/EW enterprise
  - Through integration of mission and target-specific SW applications
  - Through continual integration of next generation COTS HW technologies



**As the Technology Matures, More Systems will Adopt, Accelerating Development**





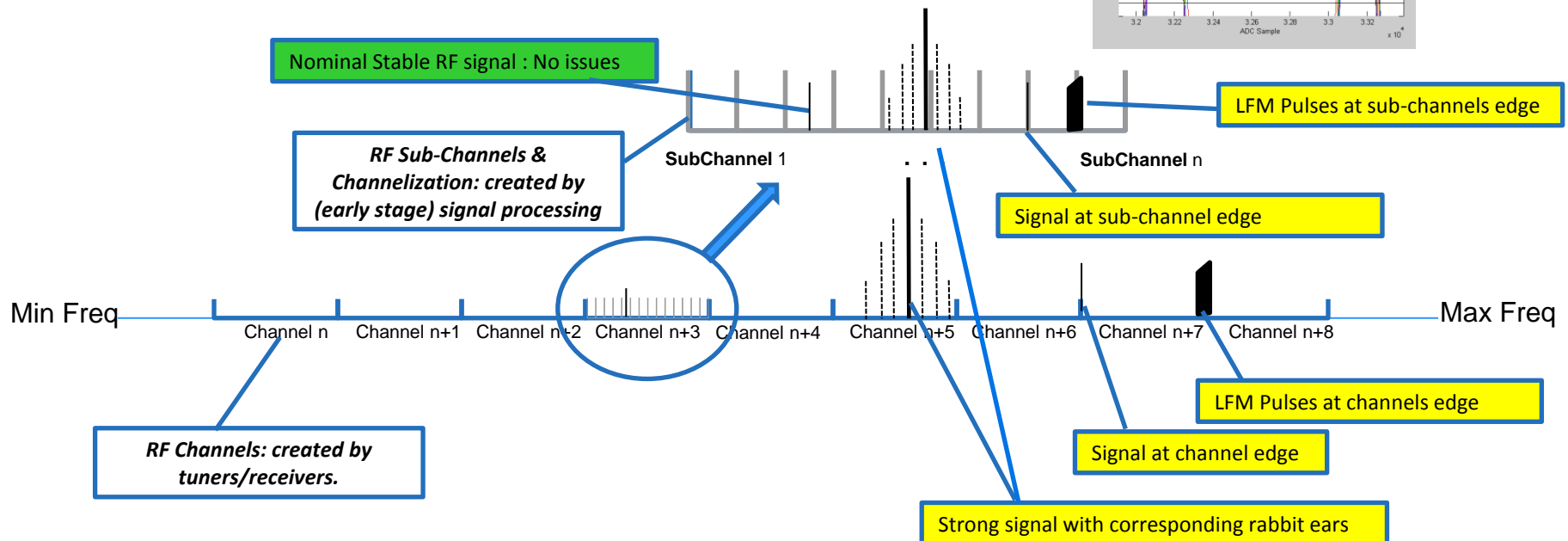
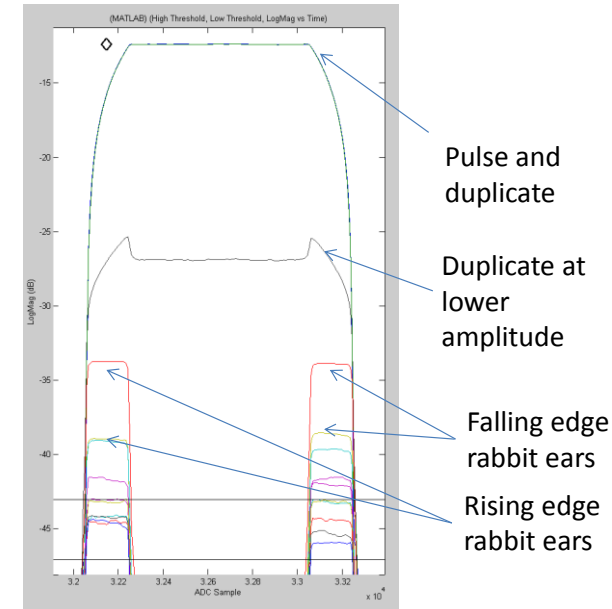
# 1.0 – Complex Pulse Measurement - Background



## Pulse Filtering and Channelizer Compensation

### Summary:

- To achieve wideband coverage, the RF spectrum is divided into channels and further sub-divided into sub-channels
- The division/sub-division of the RF spectrum creates conditions that have to be accounted for various signal types in order to accurately measure/characterize the RF environment

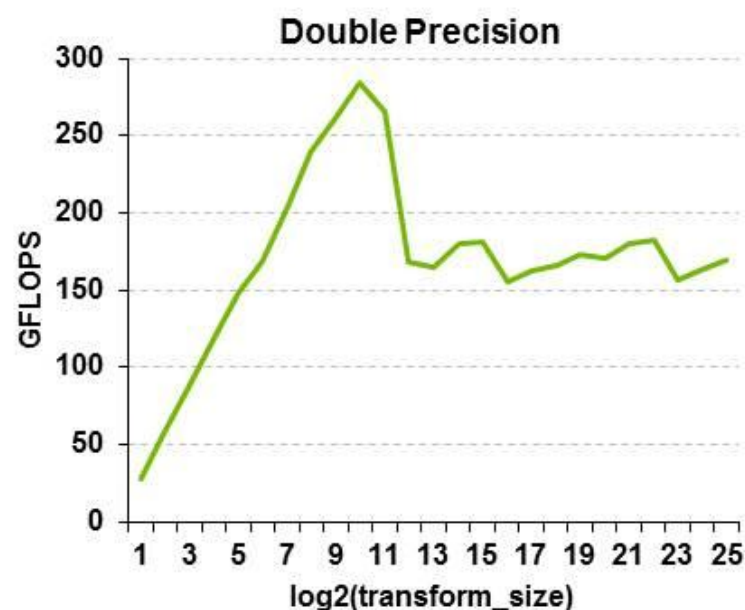
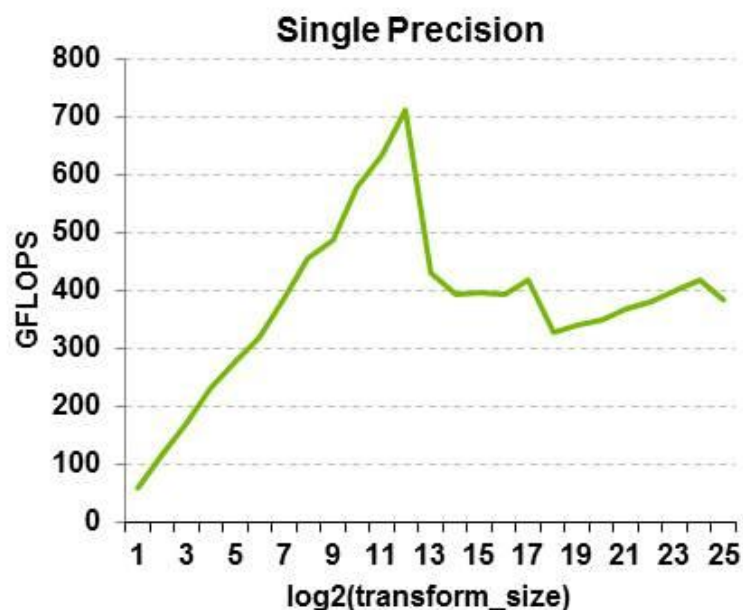




## cuFFT: up to 700 GFLOPS

1D Complex, Batched FFTs

Used in Audio Processing and as a Foundation for 2D and 3D FFTs



Performance may vary based on OS version and motherboard configuration

• cuFFT 6.0 on K40c, ECC ON, 32M elements, input and output data on device