CATEGORY: DATA CENTER, CLOUD COMPUTING & HPC - DC01 POSTER CONTACT NAME Sandeep Agrawal: sandeep@cs.duke.edu P5175



# **GPU** TECHNOLOGY CONFERENCE

	5. SpMM – Accelerator					
	<ul> <li>Partition tile</li> <li>Two step partition2</li> <li>Partition2</li> <li>Partition1</li> <li>Tiles reside</li> <li>Use scratch</li> </ul>	into m artition create create in acc pad m	hicrotile functions es para elerato emory	es at r on due allelisn allelisn or mer	Funtime to increase paralleli to PCI-E constraints in for SpMM in for Partition2 mory, avoiding PCI-E transf pre occupancy array	
	8. Experimental Setup					
	Platform	\$ <sub>fixed</sub>	\$ <sub>cpu</sub>	\$ <sub>acc</sub>	Description	
5	Xeon	4500	2300	-	PowerEdge R720, 2 x Xeon E5-26 8x8GB 1866MHz RDIMMs	
	Xeon + Titan	4500	2300	1000	PowerEdge R720, 2 x Xeon E5-26 2688 CUDA cores, 14 SMs, 6GB (	
	Xeon + Maxwell	4500	2300	150	PowerEdge R720, 2 x Xeon E5-26 640 CUDA cores, 5 SMs, 2GB GD	
	SoC + Titan	200	-	1000	J1800 SoC, 22 nm, 4GB DDR3L F	
	SoC + Maxwell	200	-	-	J1800 SoC, 22 nm, 4GB DDR3L F	
	<ul> <li>Search acros</li> <li>Queries are r</li> <li>95% latency</li> <li>Create mode consumed fo</li> <li>Pick µ and C</li> </ul>	ss the f random evalua ls for \$ r searc giving	English hly pick ited us b <sub>capital</sub> a ching a lowes	n Wikip ked fro ing Mo and \$ <sub>op</sub> and \$ <sub>op</sub> across at \$ <sub>total</sub>	bedia (Bag of words model) om page titles onte Carlo simulations berational based on number of 1 Billion documents = \$capital + \$operational	

ism per query
fers
650v2, 22 nm, 16C/32T,
650v2, GTX Titan, 28 nm, GDDR5 Memory
650v2, GTX 750Ti, 28 nm, DDR5 Memory RAM, GTX Titan
RAM, GTX 750Ti
machines and energy
Xeon+Maxwell
well 🔶 Xeon+Titan
+ Titan
40 0.60 0.80 alized to Xeon)
or T = 50 ms and eries/sec

NVIDIA and Duke University