OpenCores

Free open source IP cores and chip design

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OpenCores

What is OpenCores ?

Repository of open source, freely available Intellectual Property (IP)

- 17 mailing lists
- 276 projects
- 633 members

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OpenCores

Novas nLint is integrated into OpenCores CVS system

This new tool helps designers to write better quality HDL code by performing source code checks to ensure conformance with design rules such as synchronous design, clocking scheme, naming conventions, and testability.

We configured nLint according to OpenCores design guidelines. This way we will get common coding style for all cores stored in the CVS.

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CPU

- 32 bit architecture, ORBIS 32
- Scalar, single issue 5-stage pipeline
- Single cycle execution
- MAC 32x32
- Custom instructions

MMU

- memory management unit

L1 Caches

- I/D Cache (1 to 64 KB)

Interrupt controller

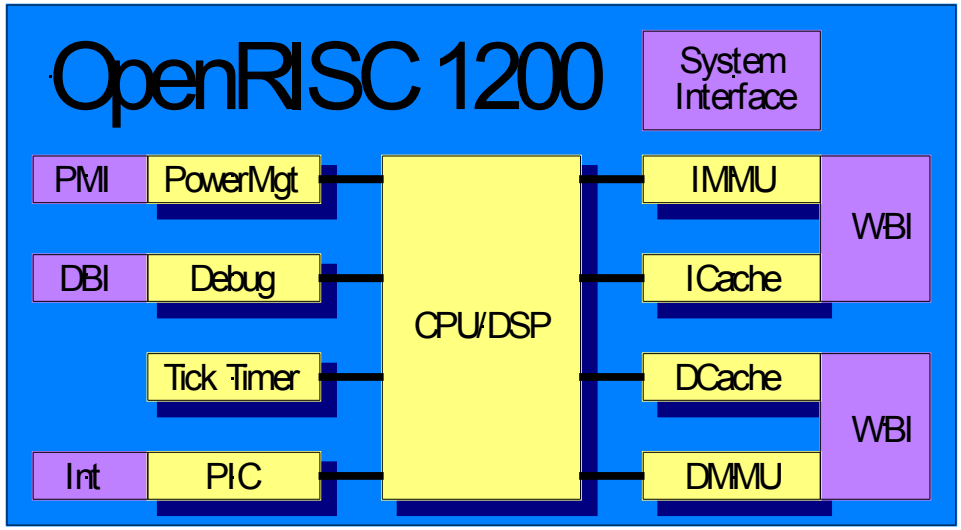
- 30 maskable interrupt sources

Tick timer

- Task scheduling

Debug Unit

- JTAG test access port



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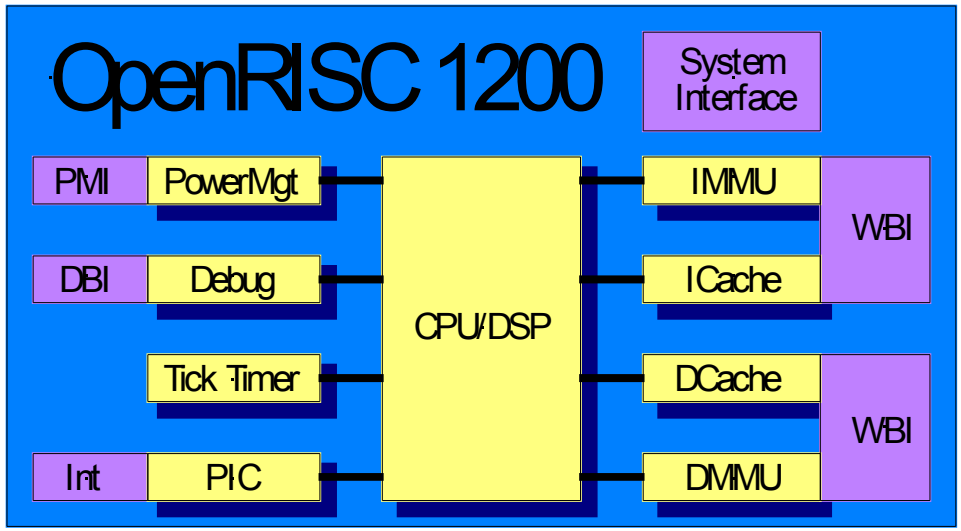
TUTORIALS on the OpenRISC implementation on Xilinx and Altera FPGA boards. Very useful for beginners, a must read for everyone wanting to implement OpenRISC based system on a FPGA for the first time.

Also features tutorial how to build the OpenRISC GNU toolchain.

Credits go to Resarch Group Digital Techniques, Hogeschool voor Wetenschap & Kunst.



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OpenRISC 1000: Linux

Linux is a free, open source UNIX kernel that together with the GNU C library and GNU utilities forms the GNU/Linux operating system.

- Free, open source code with no royalty
- UNIX class operating system
- Process protection through use of the Memory Management Unit
- Multitasking, preemptive scheduling
- Interprocess communication and synchronization
- TCP/IP networking and numerous other network protocols
- File systems NFS, ext2, MS-DOS, FAT16/32 and others

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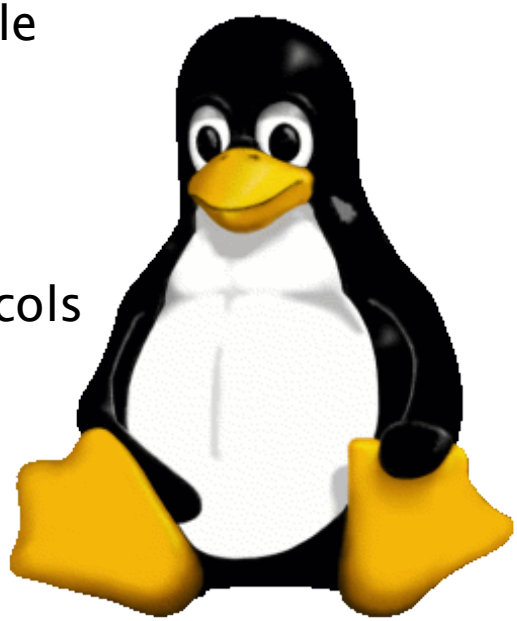
OpenRISC 1000: uCLinux

uClinux is a derivative of Linux kernel intended for microcontrollers without Memory Management Units (MMUs).

- Free, open source code with no royalty
- small code footprint suitable for embedded and portable applications
- common Linux API
- Multitasking, preemptive scheduling
- high performance C libraries with small footprint
- TCP/IP networking and numerous other network protocols
- File systems NFS, ext2, MS-DOS, FAT16/32 and others



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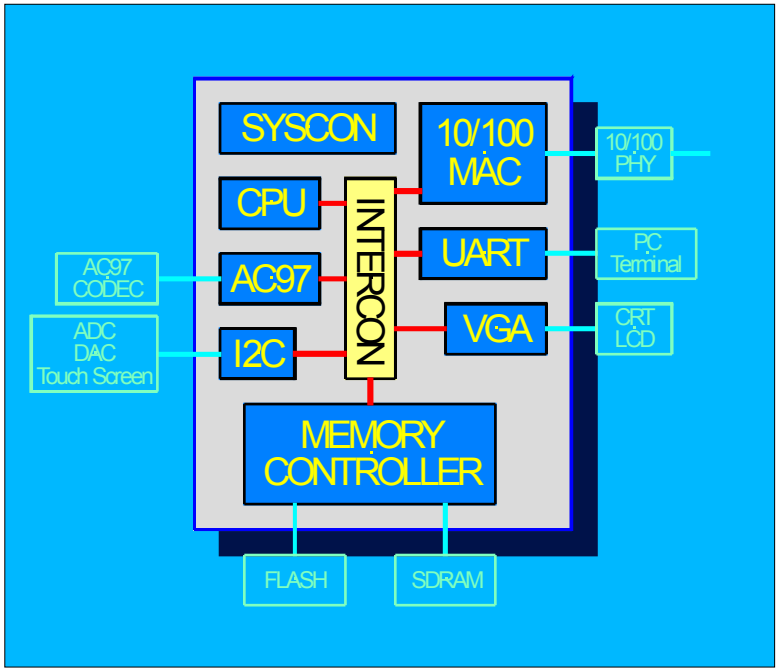
WISHBONE
System-on-Chip interconnect architecture

- Open specification
- Patent and royalty free
- Multi-master, Mulit-Slave
- Interconnect independent
- Synchronous bus
  All signals are triggered on the rising edge of the system clock



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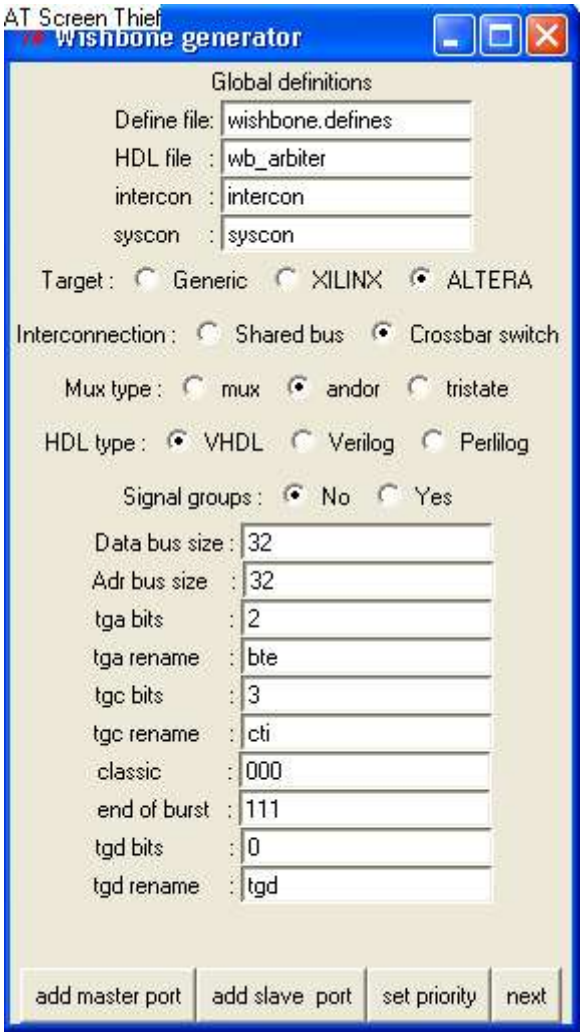
WISHBONE
System-on-Chip generator

- Generates HDL (VHDL/Verilog) for wishbone implementations
- Priority handling
- Shared bus or crossbar switch
- Written in PERL/Tk



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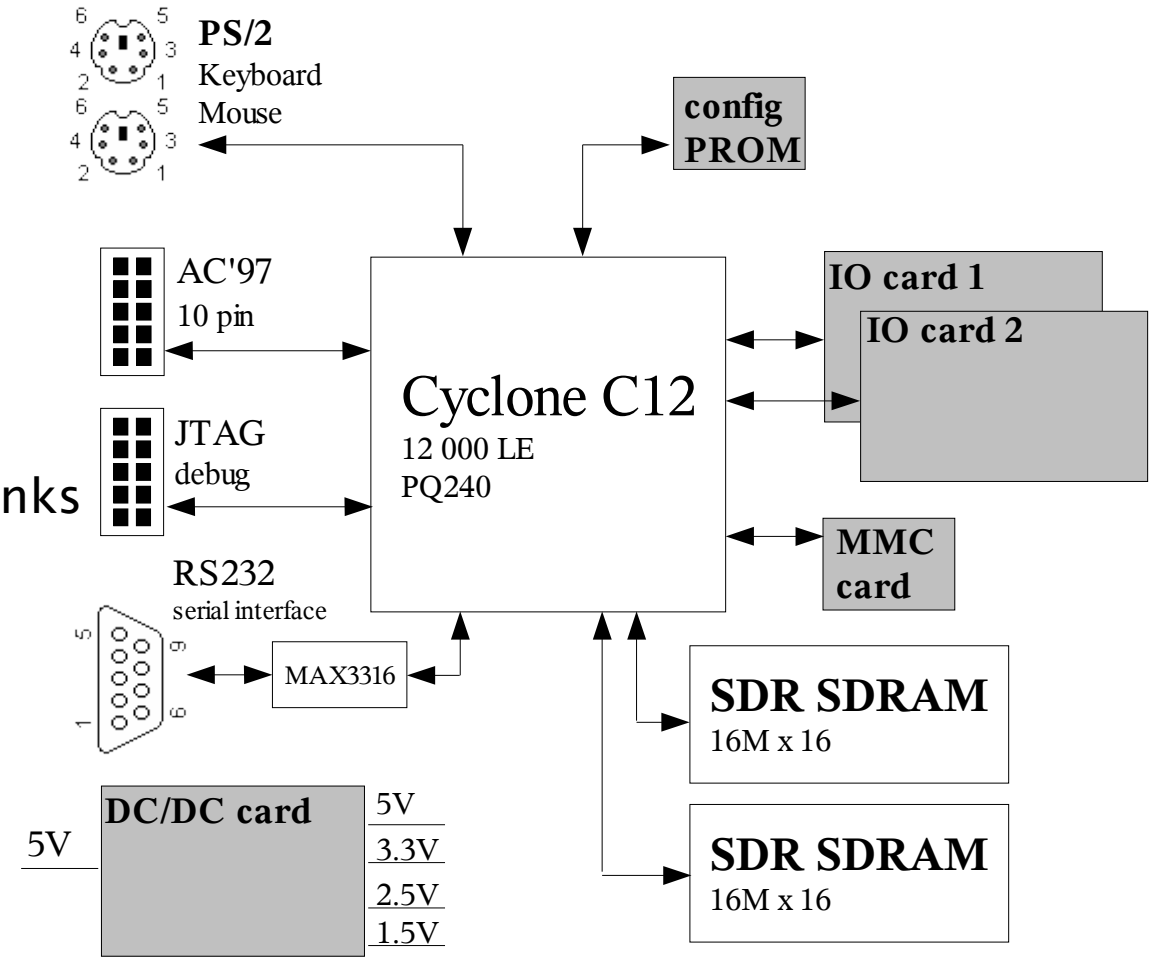
SoC

development board

- Optimized for OpenRISC
- ALTERA Cyclone C12
- Two independent SDRAM banks
- Ethernet 10/100 card
- VGA card



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MARVIN – Flextronics Semiconductor implementation

- UMC 0.18um
- OR1200 processor
  - 8KB data cache
  - 8KB instruction cache
  - 32x32 mult, 64-bit MAC
- Memory controller
- PCI 2.2 32-bit interface 33/66 MHz
- Ethernet MAC 10/100
- UART16550
- GPIO
- JTAG/debug interface
- SoC clock frequency 160 MHz

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New IP cores

- Tiny64

  A simple 64-bit microprocessor in VHDL. The wordsize of TinyX is configurable via constant XLEN in TinyXconfig.vhd from 32 bit in 8 bit steps upto the gatearray limit. A simple assembler is also included (wordsize configurable).

- JOP

  JOP is the implementation of the Java Virtual Machine (JVM) as concrete machine in hardware. The design has been sucessfully implemented in low cost FPGA devices from Altera (ACEX 1K50, Cyclone) and Xilinx (Spartan II).

  about 2000 LCs in Altera FPGA
  fmax is 100 MHz on a Cyclone EP1C6

- perlilog

  Perlilog is a design tool, whose main target is easy integration of Verilog IP cores for System-on-Chip (SoC) designs. At a smaller scale, Perlilog is a great starting point for writing scripts which handle Verilog code in general. It comes with a rich set of functions, that can be used for several purposes, such as instantiation of ASIC pads, automatic connection and generation of simple Verilog modules, and so on.

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open source hardware

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