MDE based FPGA physical Design
Fast prototyping with Smalltalk

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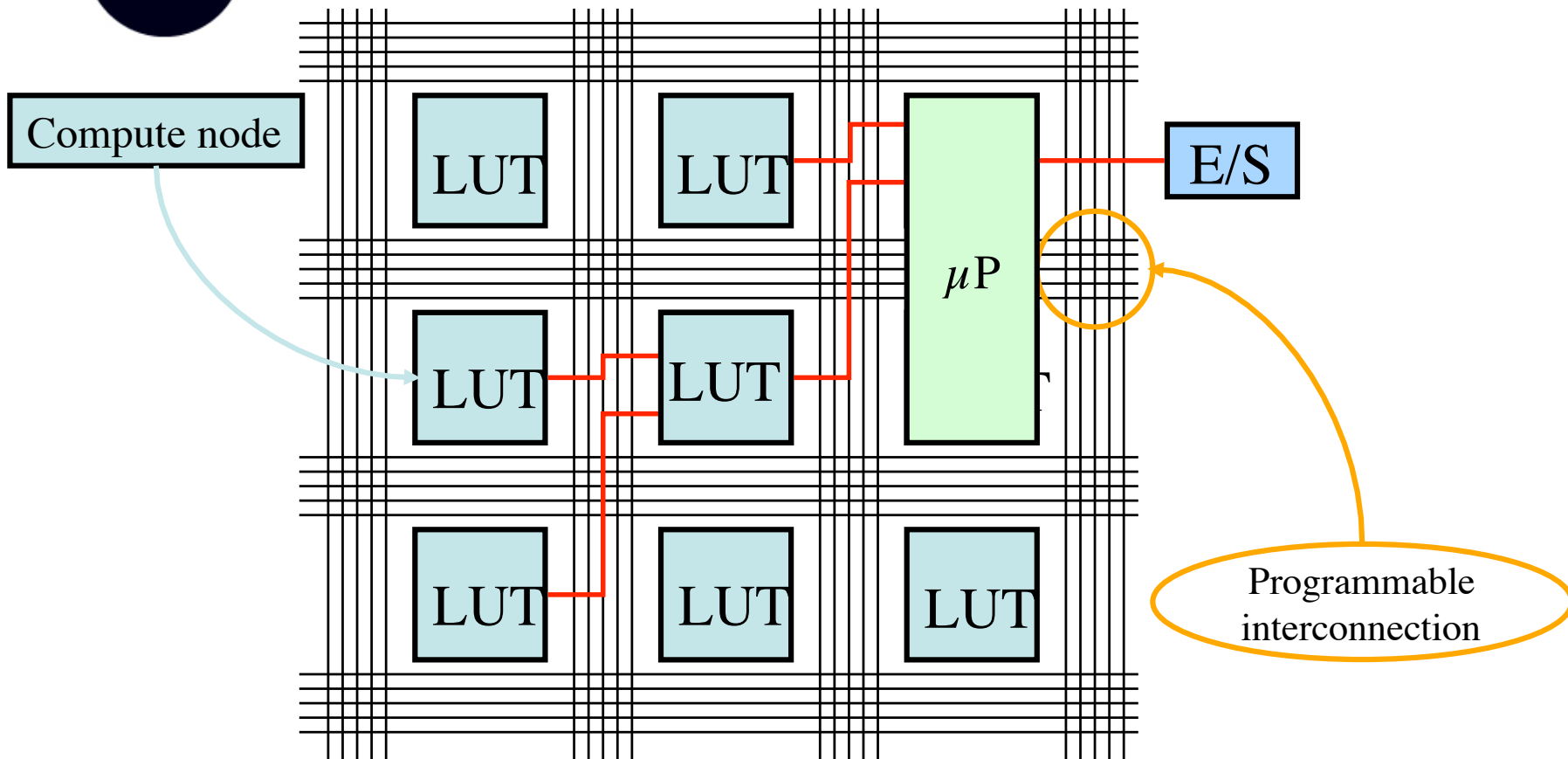L'Université est une chance

FPGAs

"Flexible" hardware
Time to market

Hard to program
Hard to debug

Compute node

LUT	LUT	μP
LUT	LUT	
LUT	LUT	LUT

E/S

Programmable interconnection

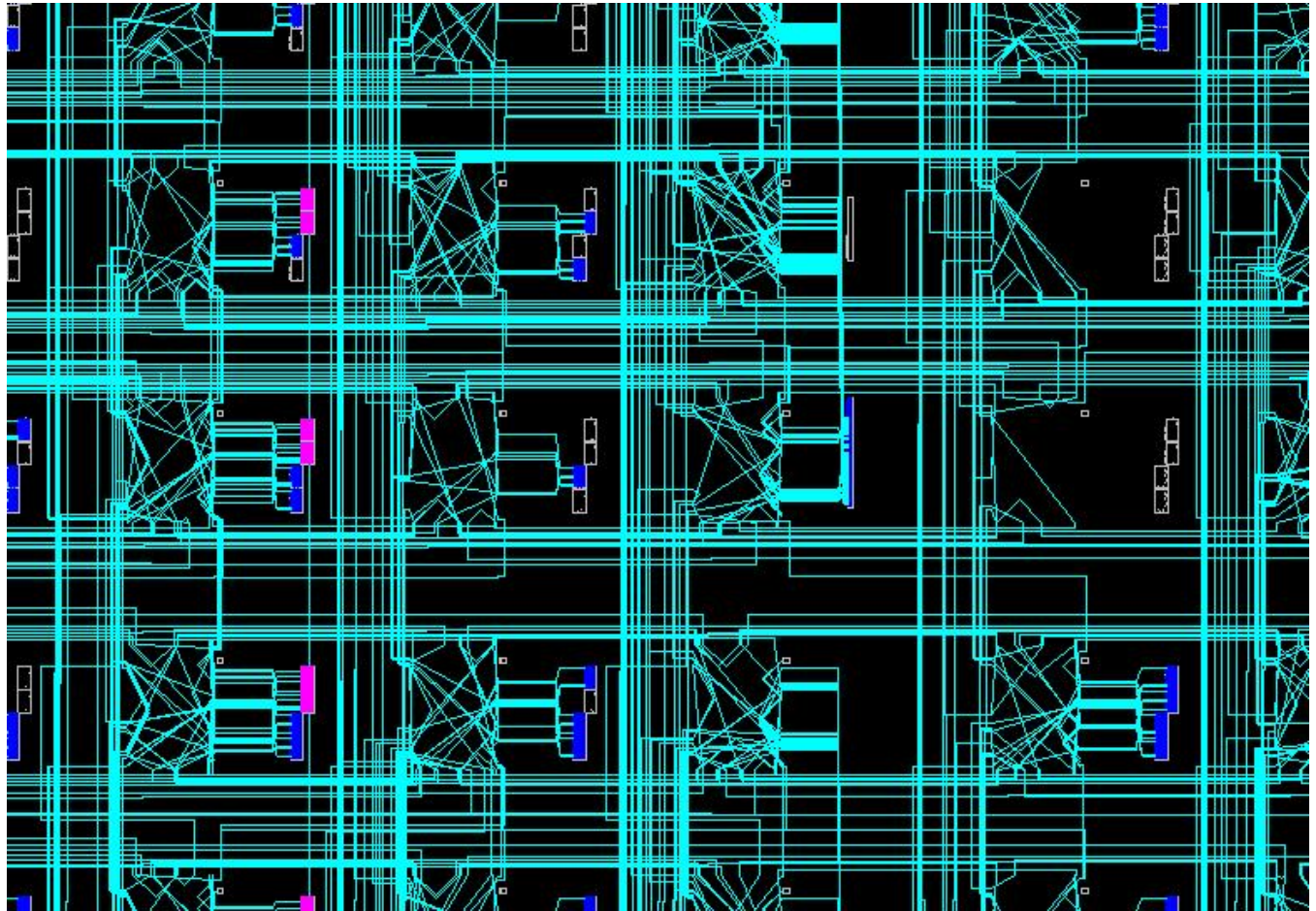L'Université est une chance

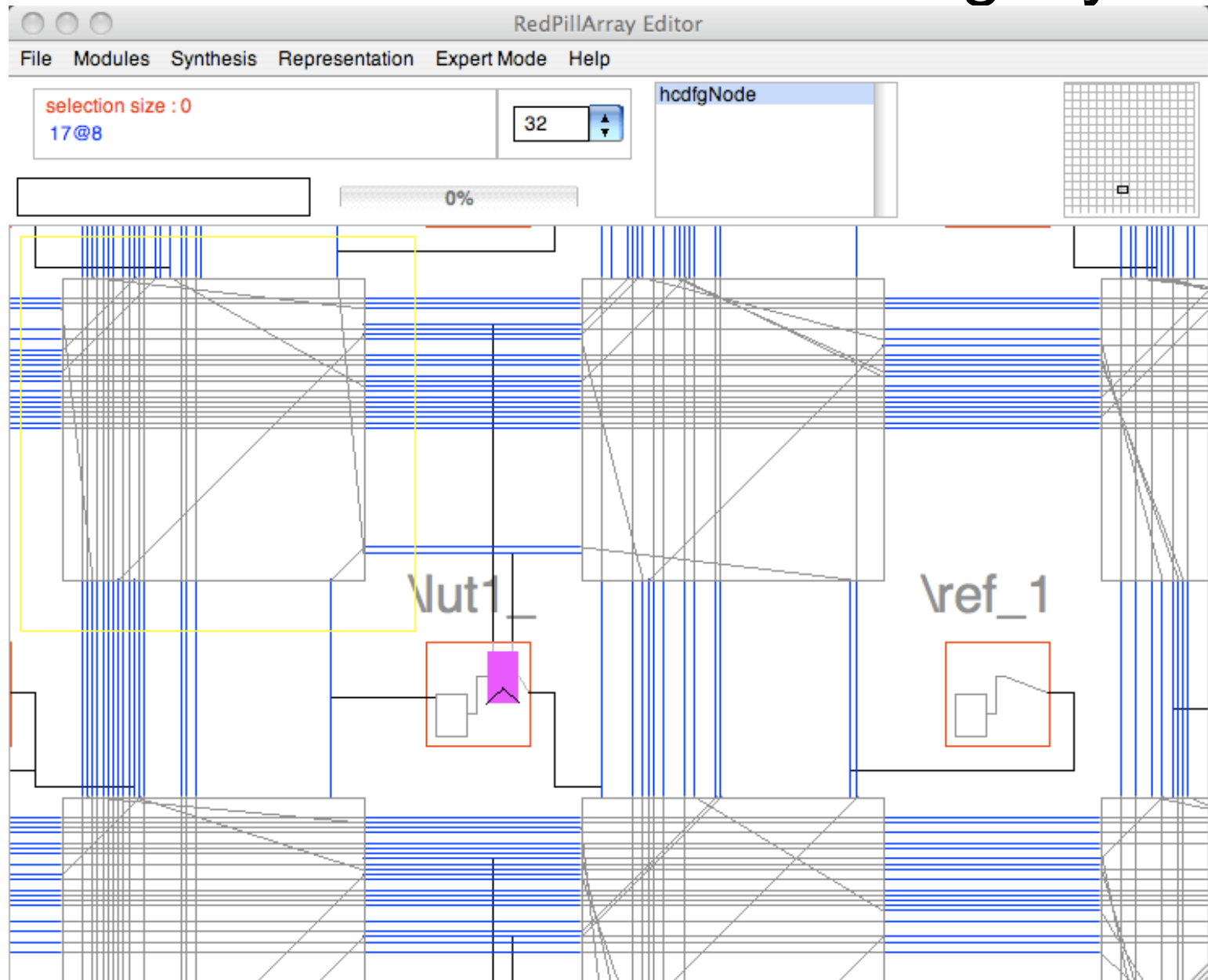# FPGAs

+ "Flexible" hardware
Time to market

— Hard to program
Hard to debug

EDA required !

- C to circuit

- Debug

- Benchmarking

Our Smalltalk-based EDA legacy

Legacy backfires

- Early developments (MADEO) started in 1996

- Fast evolving domain (Moore + Murfy)

- Refactoring is not enough to keep in the race

- We have to re-design our framework

New direction

- We need to shift from
  - a generic solution to be tailored on demand
- To
  - a repository of model, algorithms, components
- In order to deliver
  - Performances
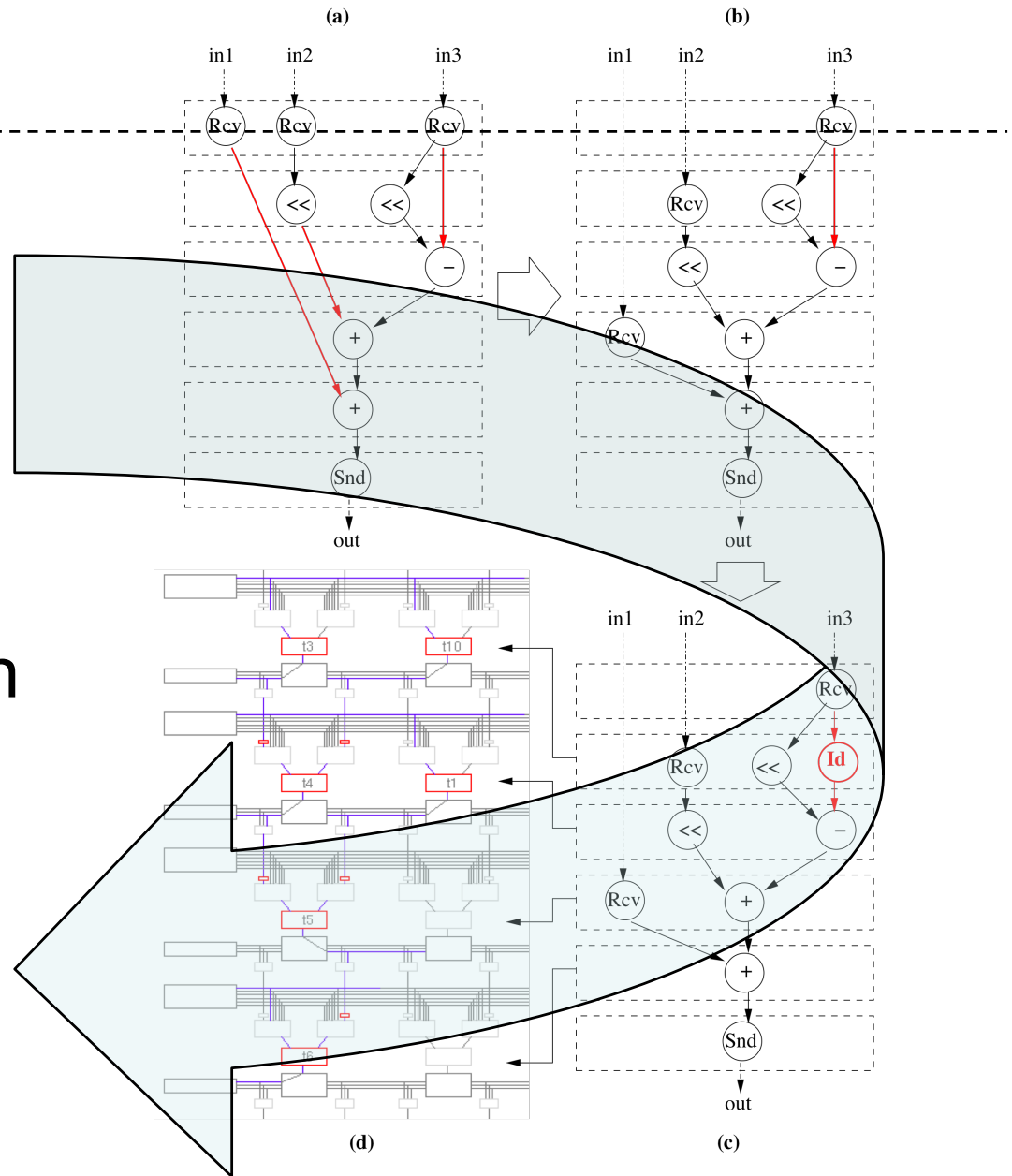 - Scalability
  - Flexibility
  - Durability

LEGACY

Front end

C code

- High level synthesis (compilation)

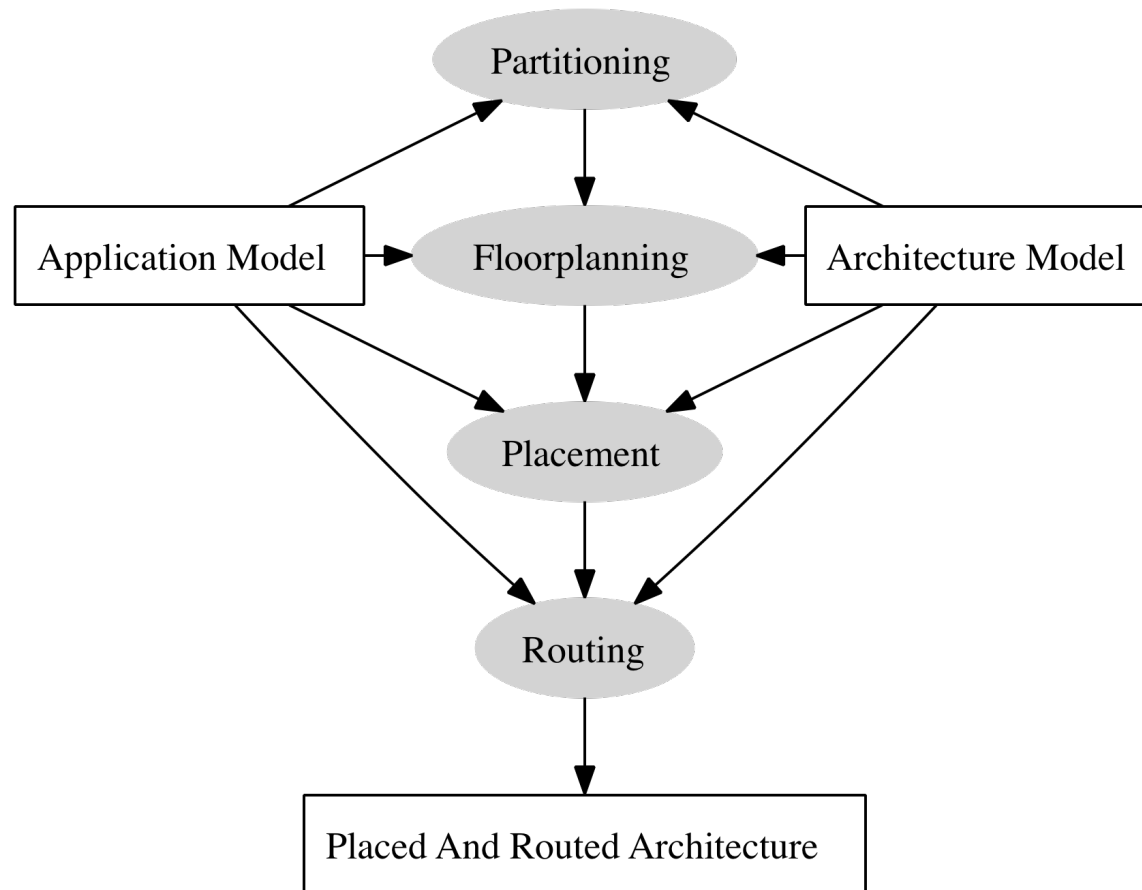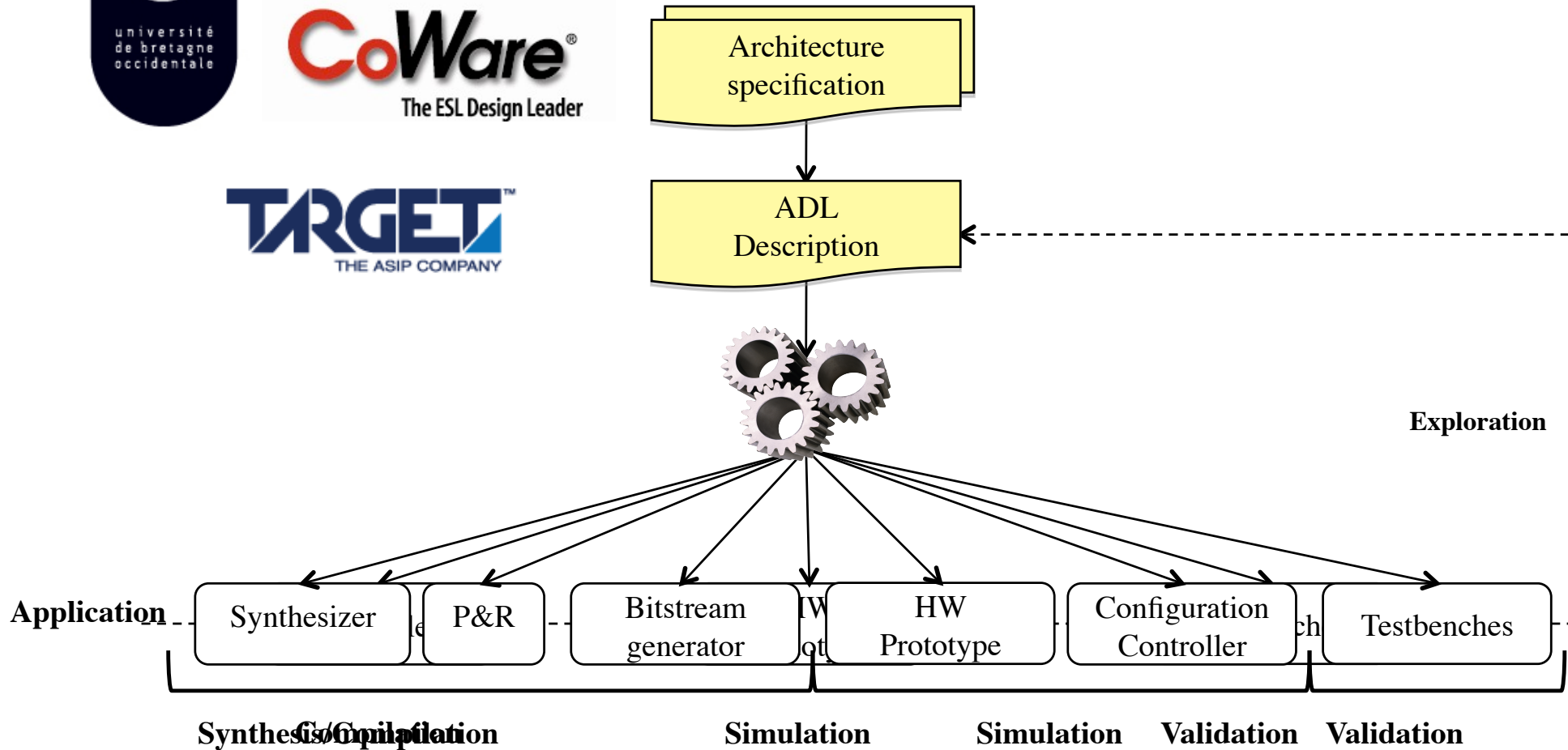- Ressources allocation (logic synthesis)

Circuit

Programming an FPGA in 4 steps
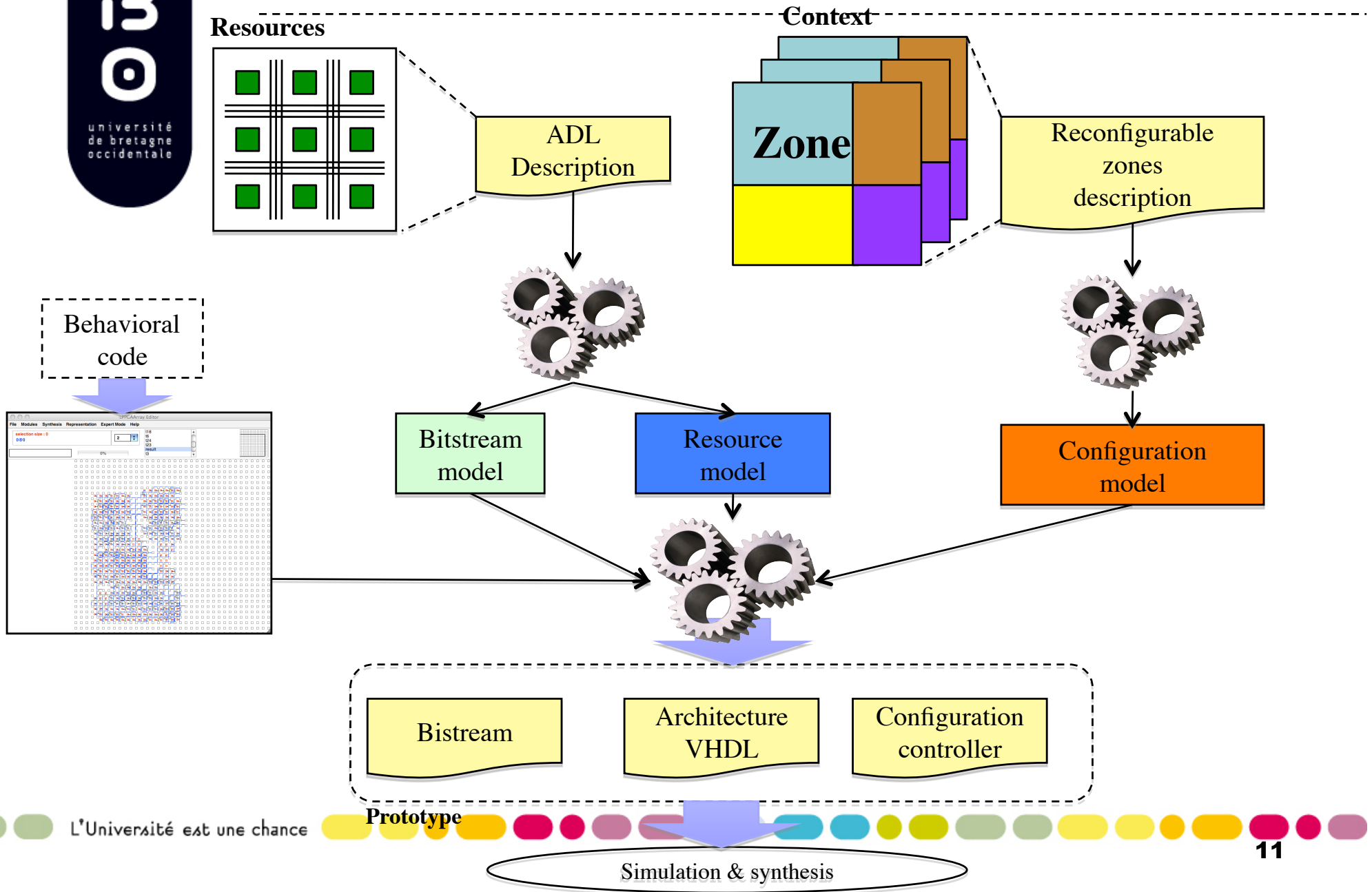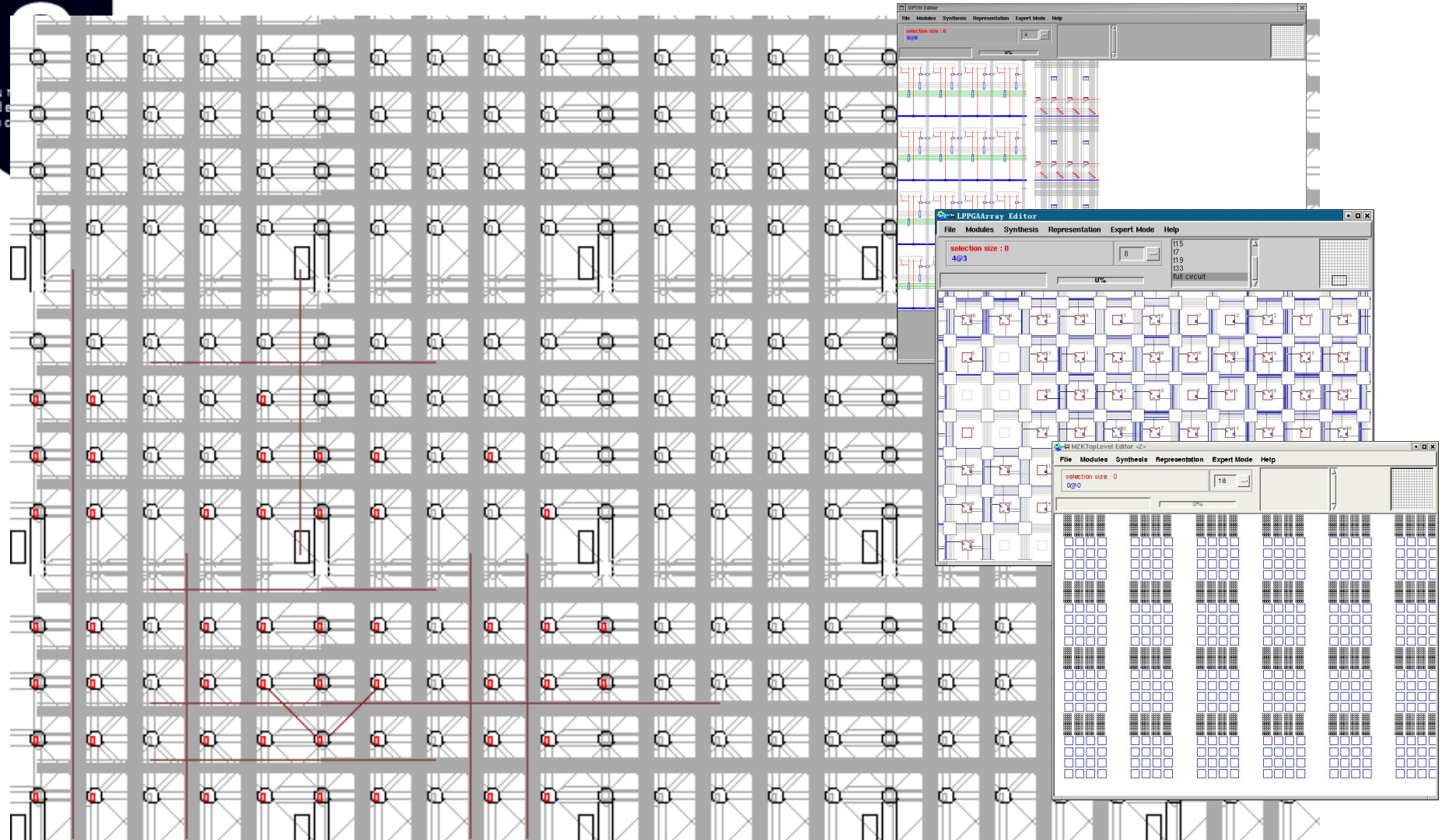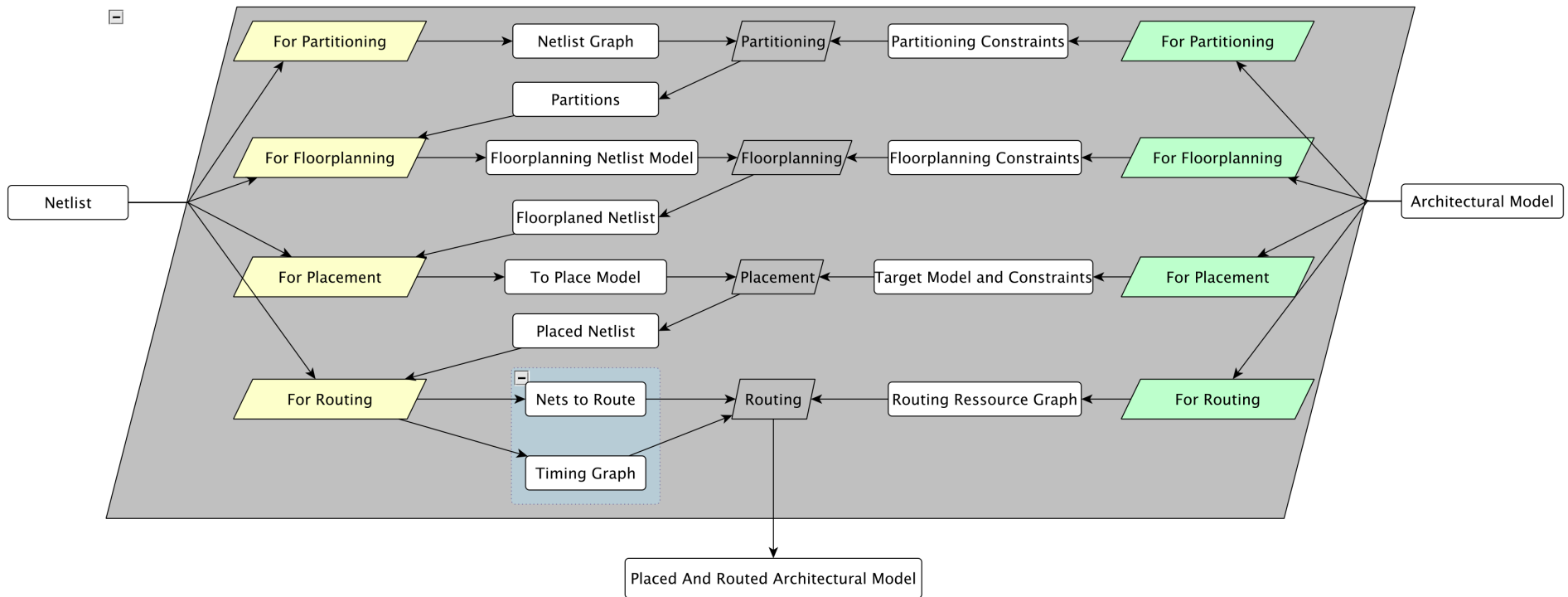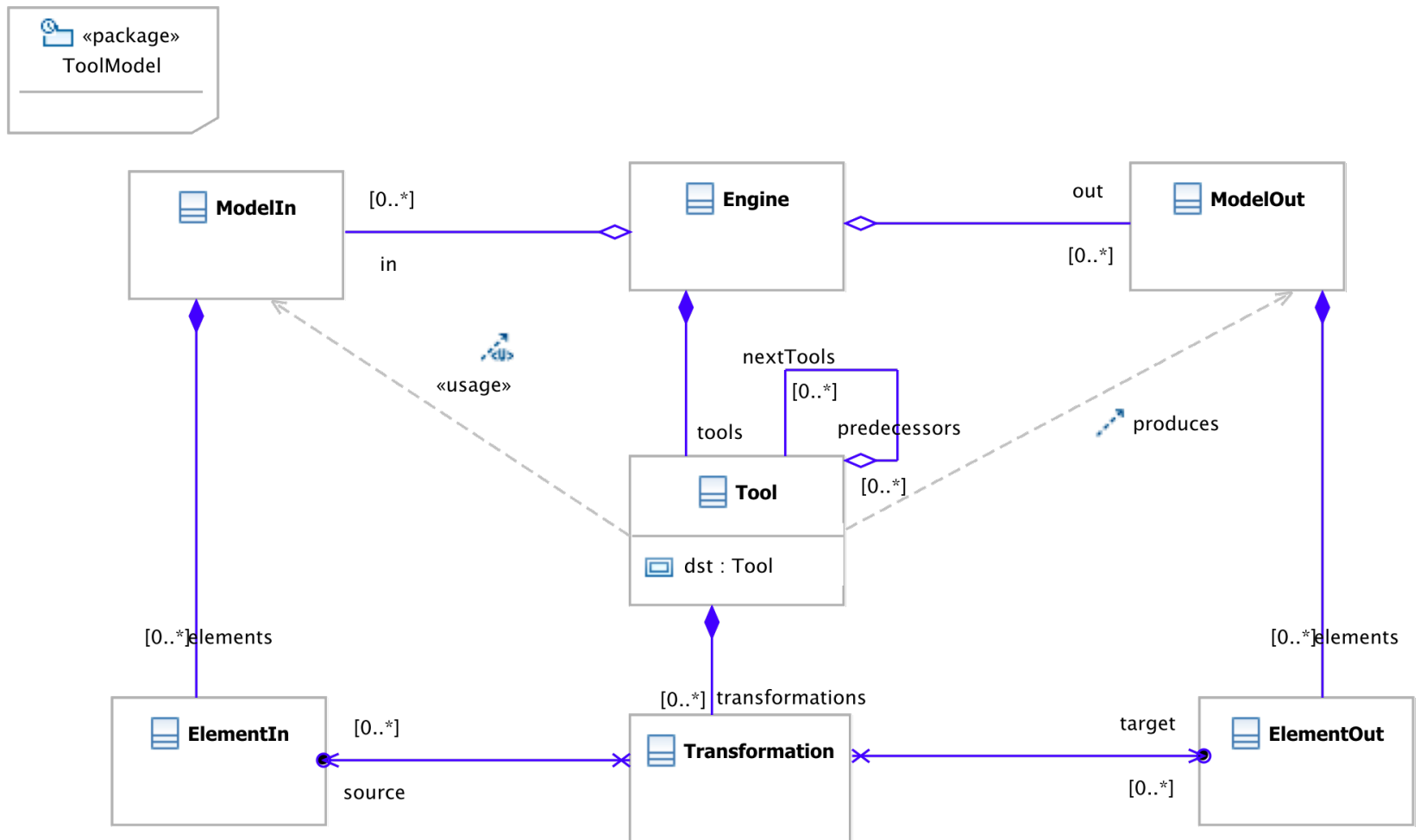
ADL Based EDA generators

Our flow

Some examples

RE-DESIGN
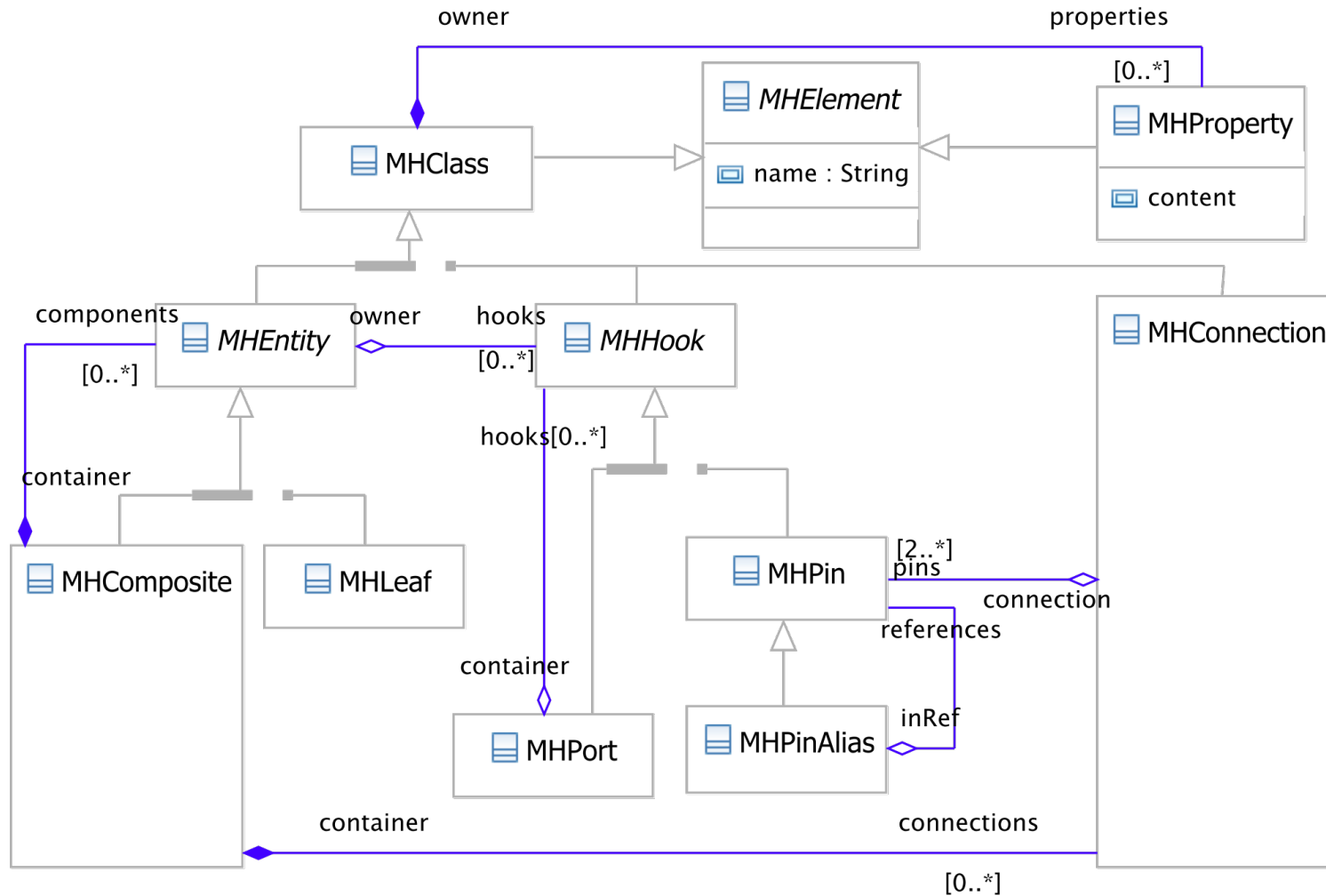
Goal oriented view extraction

Tool engine

«package»
ToolModel

ModelIn [0..*] Engine out ModelOut

in [0..*]

«usage»

nextTools
[0..*]

tools predecessors

Tool

dst : Tool

produces

[0..*]elements [0..*]elements

[0..*] transformations

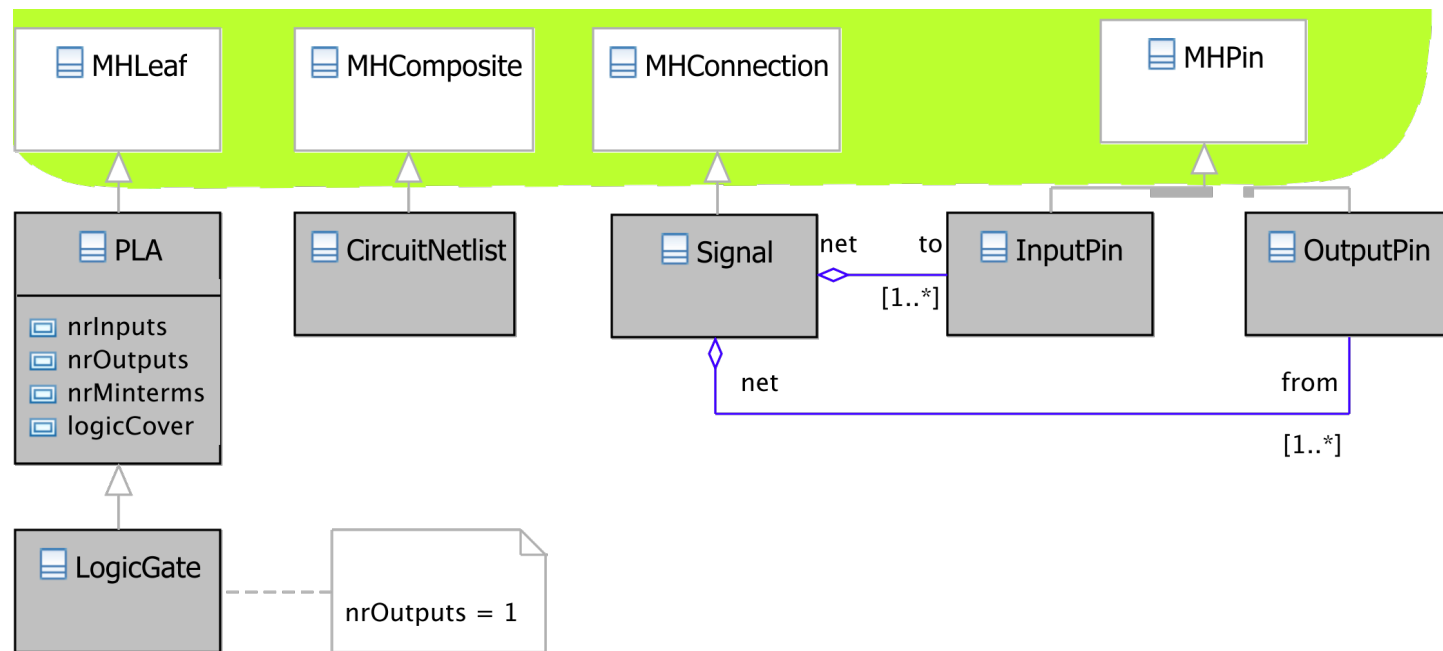ElementIn [0..*] Transformation target ElementOut
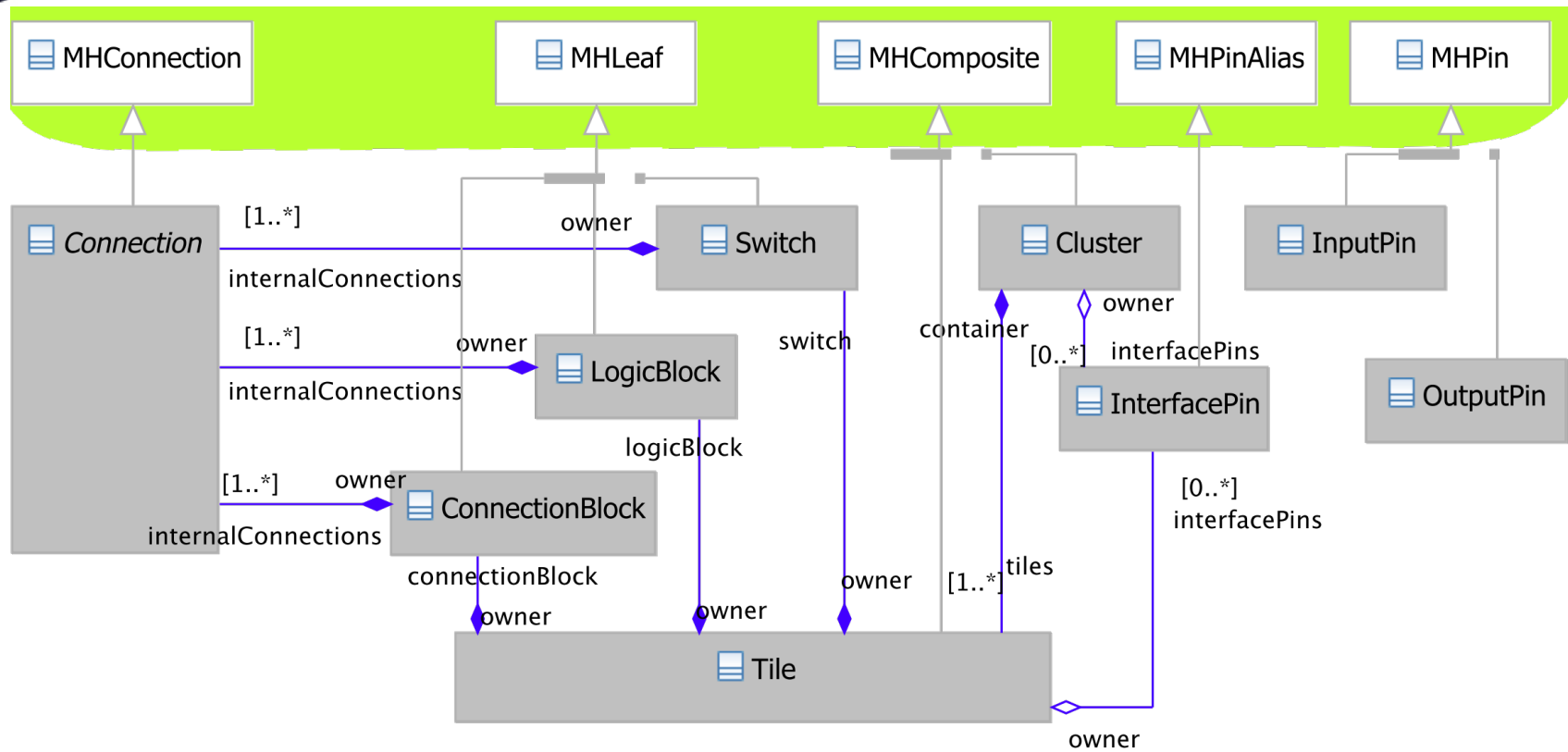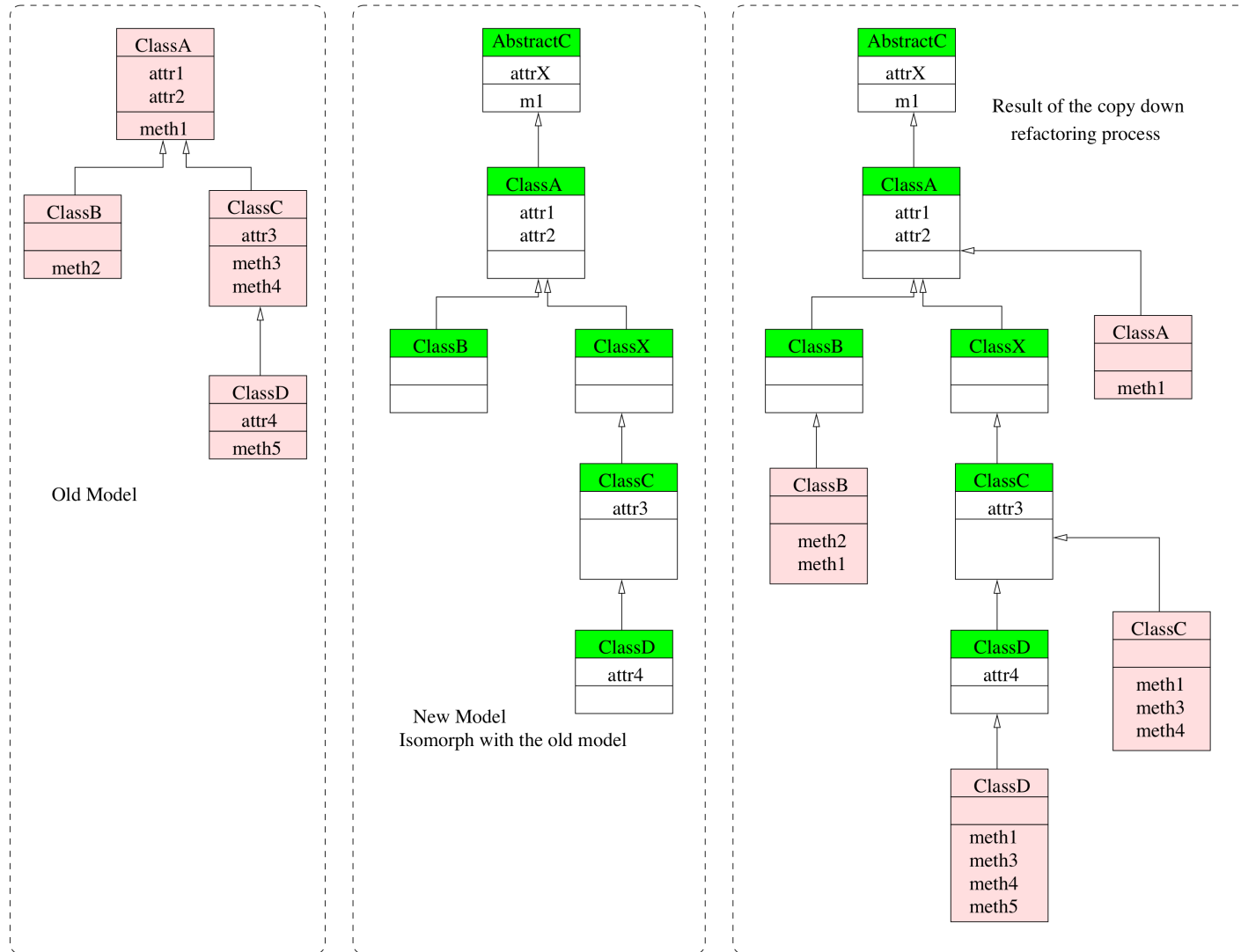
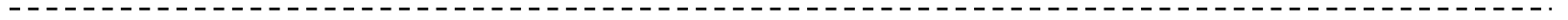source [0..*]

Models as common vocabulary

Combinational circuit modeling

Target modeling

Re-design / copy down

Old Model

New Model
Isomorph with the old model

Result of the copy down
refactoring process

CONCLUSION

Let's try to summarize

- Succes: target, tool flow

Blif

Sis

PLA Family Exploration

PLAMap

Architecture

Madeo

Placement → Routing
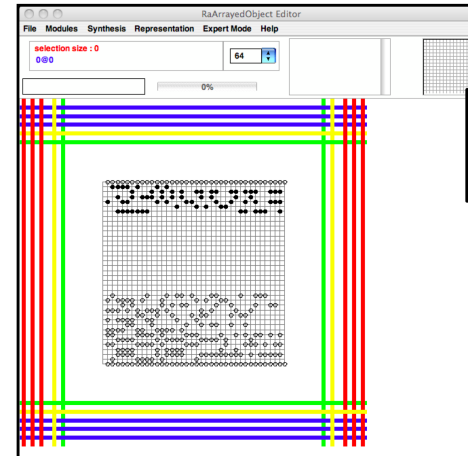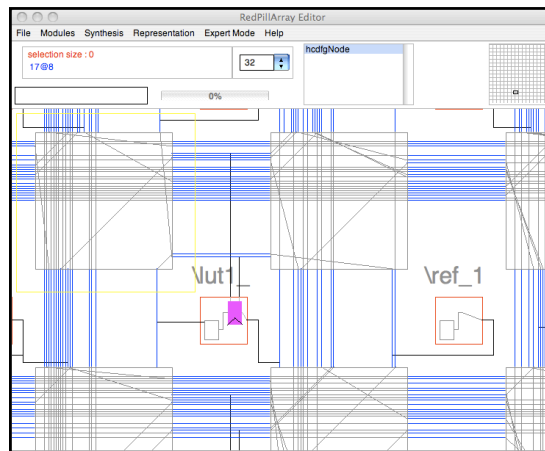
Metrics

no

yes

Layout
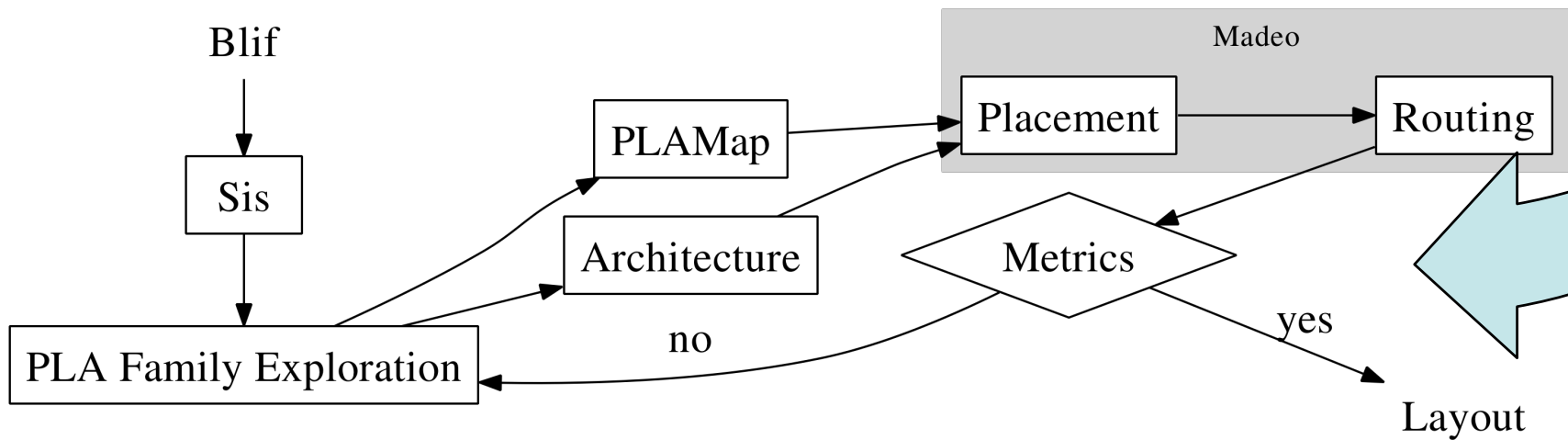
Conclusion

- Future work:
  - Tools integration (eg Mondrian integration)
  - Performances improvement
  - Test coverage
  - Algorithm pick and play GUI

Thank you for your attention